

# EE 435

## Lecture 44

Over Sampled Data Converters

Output Stages in Op Amps (slides only)

# Final Exam:

Scheduled on Final Exam Schedule:

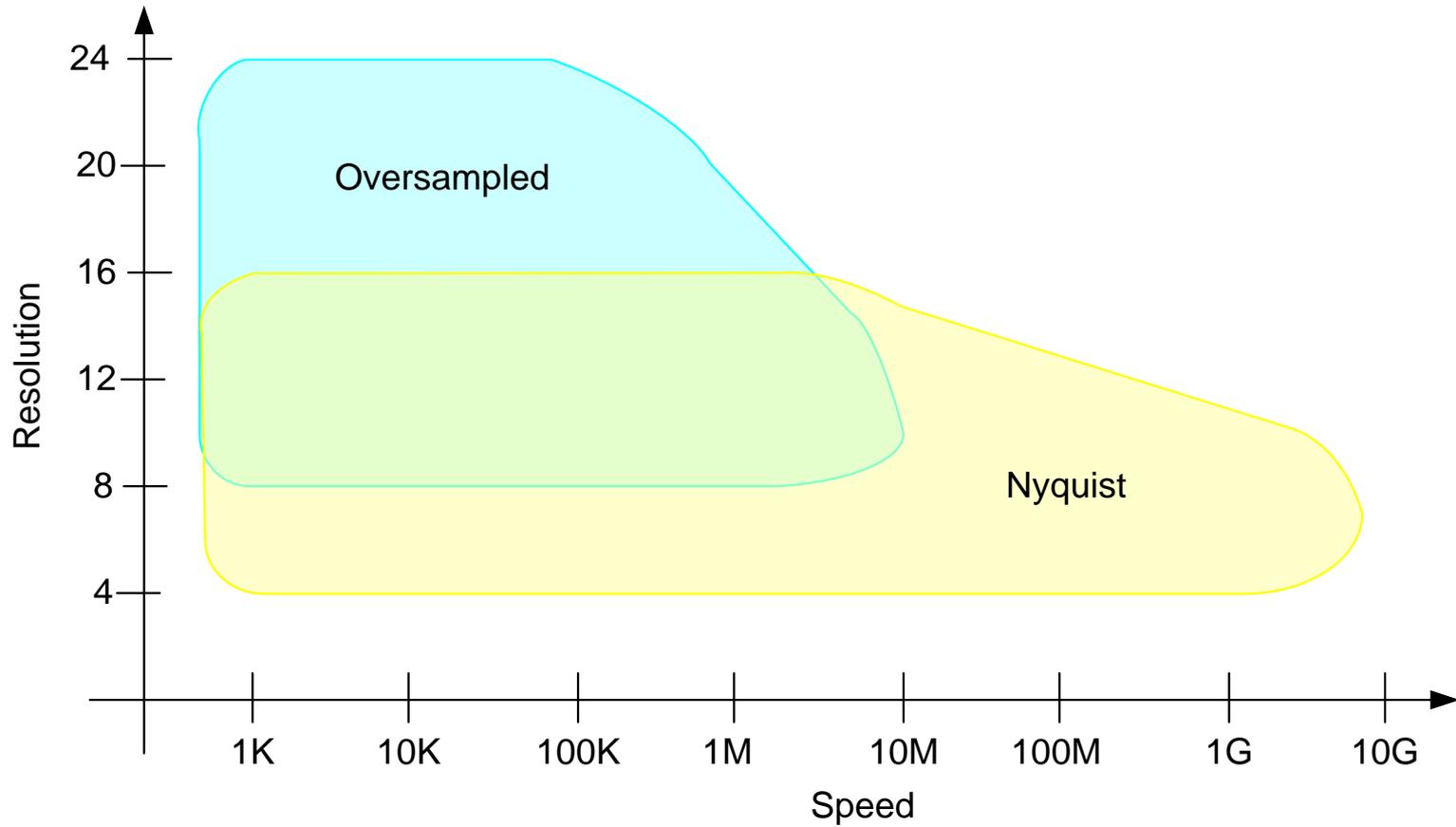
Wednesday May 14 7:30 a.m.

Revised Final Exam:

- Take-home format – open book and open notes
- Will be posted on course WEB site by Wednesday May 7
- Due at 9:30 a.m. on Wednesday May 14 : Provide hard copy and a backup solution as a pdf file in Canvas
- Honor system – students must agree to not discuss the exam with anyone except the course instructor or TA, not post or distribute the exam to any third party, and not use any outside resources (such as Chegg) for solving any problems on the exam.

If anyone has any constraints that makes it difficult to work with this revised format or would like to do an in-person exam from 7:30 to 9:30 on May 14, please contact Professor Geiger by 5:00 p.m. on Wednesday May 7

# Data Converter Type Chart

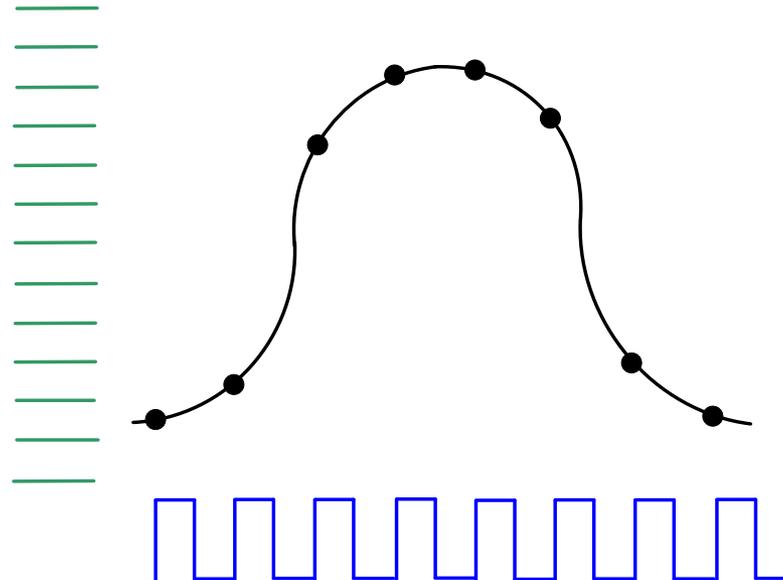
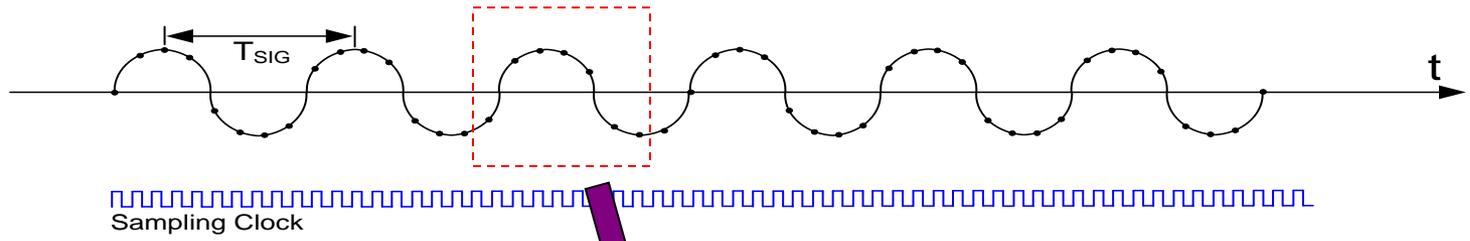


# Oversampled Data Converters

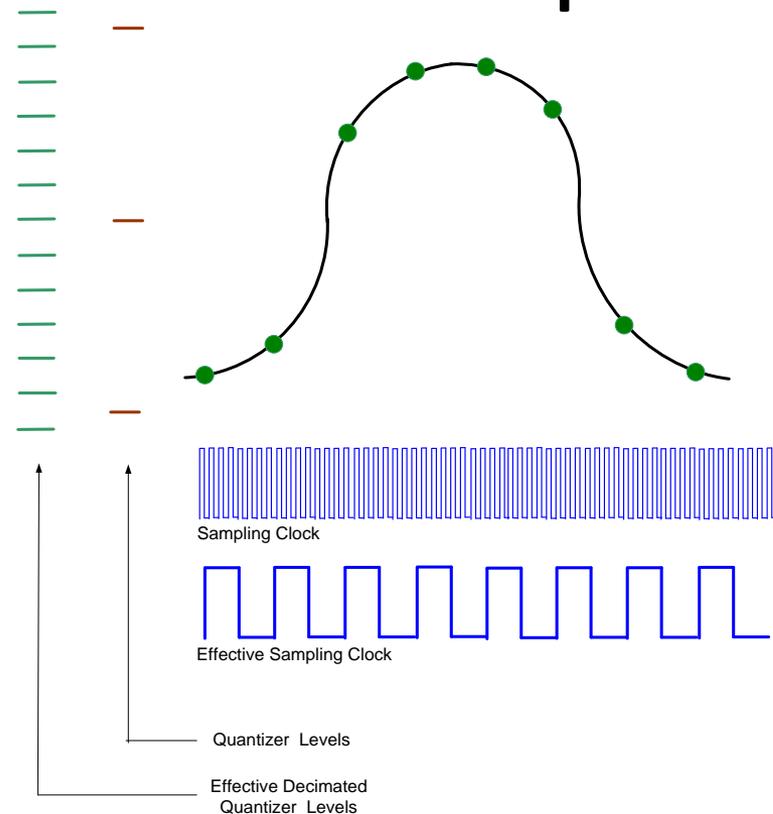
## General Classes

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

# Nyquist Rate



# Oversampled



**Oversample Ratio: Ratio between actual sampling rate and Nyquist Sampling Rate**

- Over-sampling ratios of 128:1 or 64:1 are common in oversampled data converters
- Dramatic reduction in quantization noise effects
- Limited to relatively low frequencies

Recall:

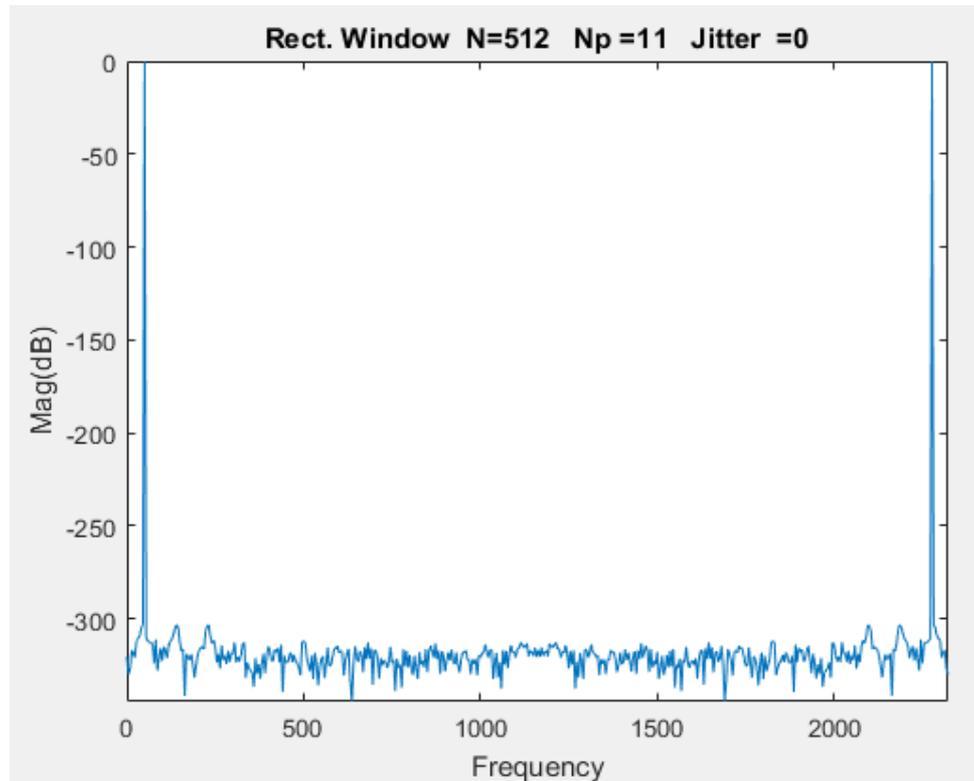
$f_{\text{SIG}}=50\text{Hz}$

$f_{\text{NYQ}}=100\text{Hz}$

$f_{\text{SAMP}}=2.3\text{KHz}$

Oversampled: 23:1

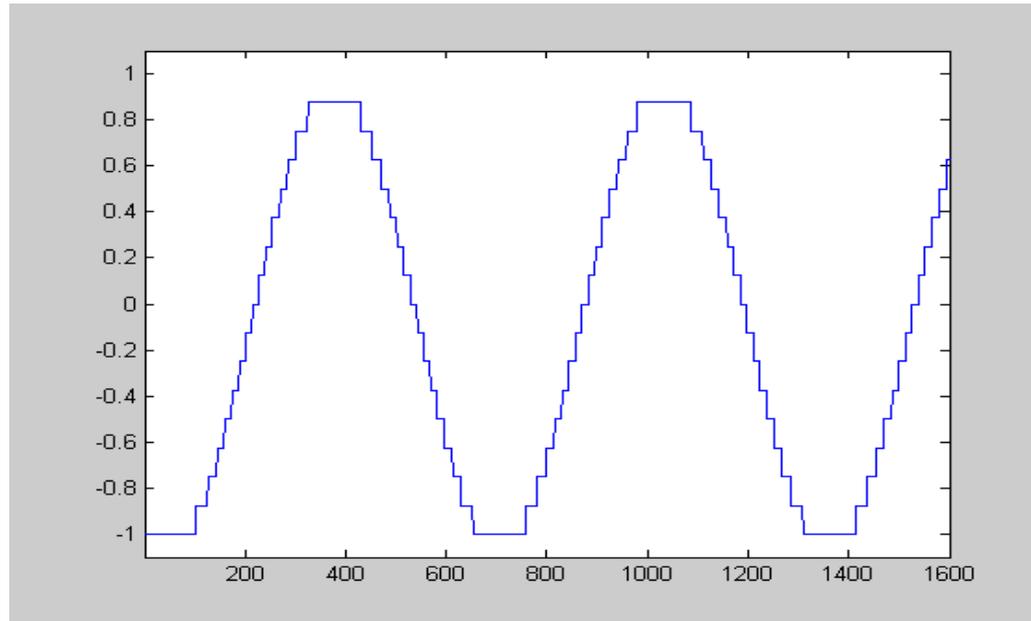
Infinite Resolution



MatLab Results

Recall:

# Quantization Effects



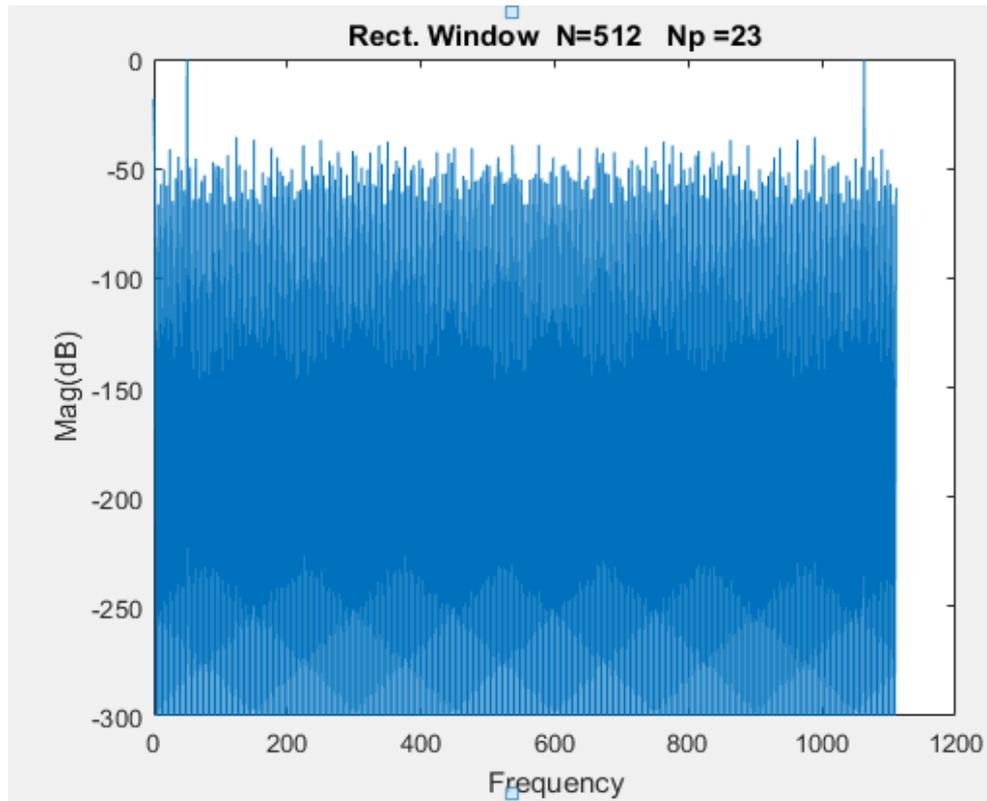
**Simulation environment:**

$$N_p=23$$
$$f_{\text{SIG}}=50\text{Hz}$$

Recall:

# Quantization Effects

Res = 4 bits



$f_{\text{SIG}}=50\text{Hz}$   
 $f_{\text{NYQ}}=100\text{Hz}$   
 $f_{\text{SAMP}}=1113\text{KHz}$   
Oversampled: 11:1

RMS Quantization Noise:

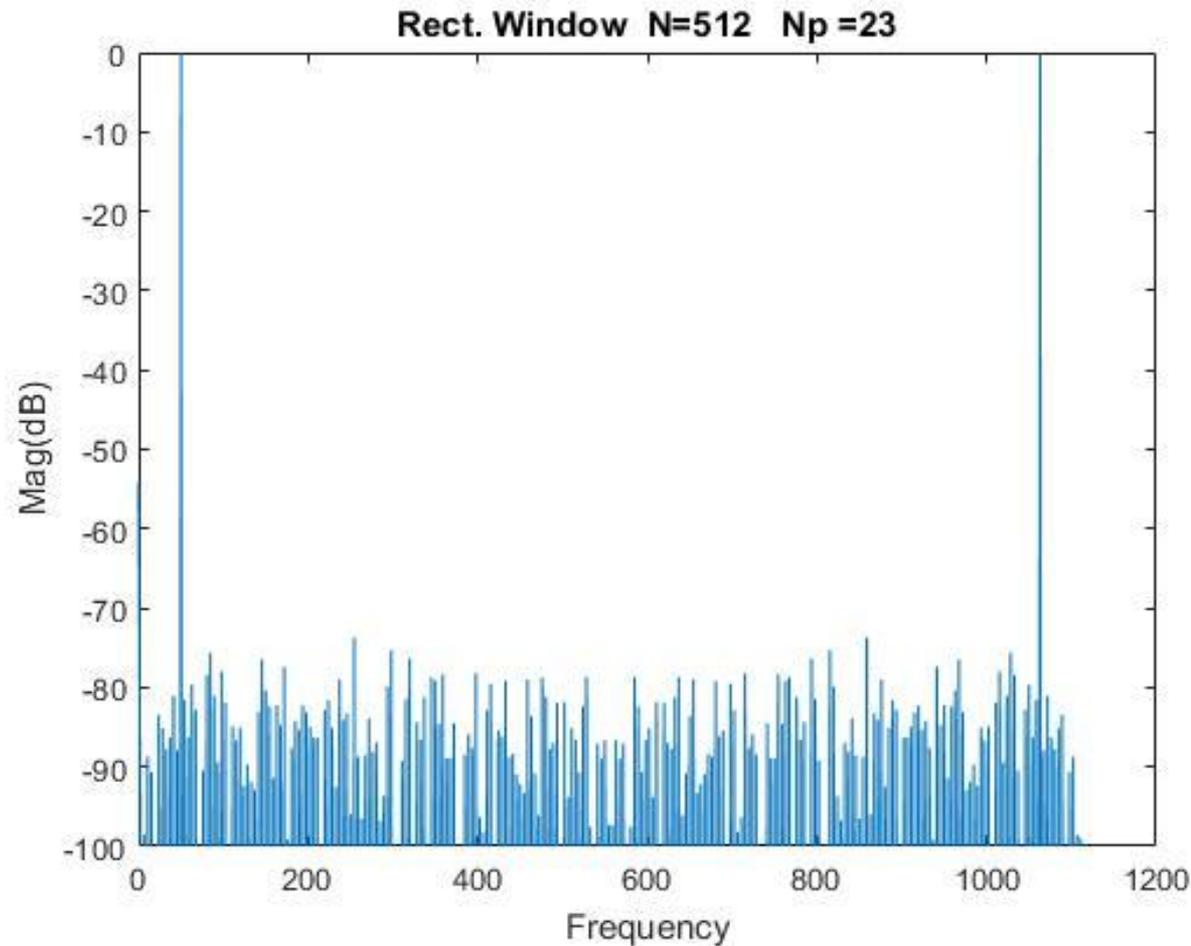
$$E_{\text{RMS}} = \frac{x_{\text{LSB}}}{\sqrt{12}}$$

Lets now increase resolution

Recall:

# Quantization Effects

Res = 10 bits



$f_{\text{SIG}}=50\text{Hz}$   
 $f_{\text{NYQ}}=100\text{Hz}$   
 $f_{\text{SAMP}}=1113\text{KHz}$   
Oversampled: 11:1

$$E_{\text{RMS}} = \frac{x_{\text{LSB}}}{\sqrt{12}}$$

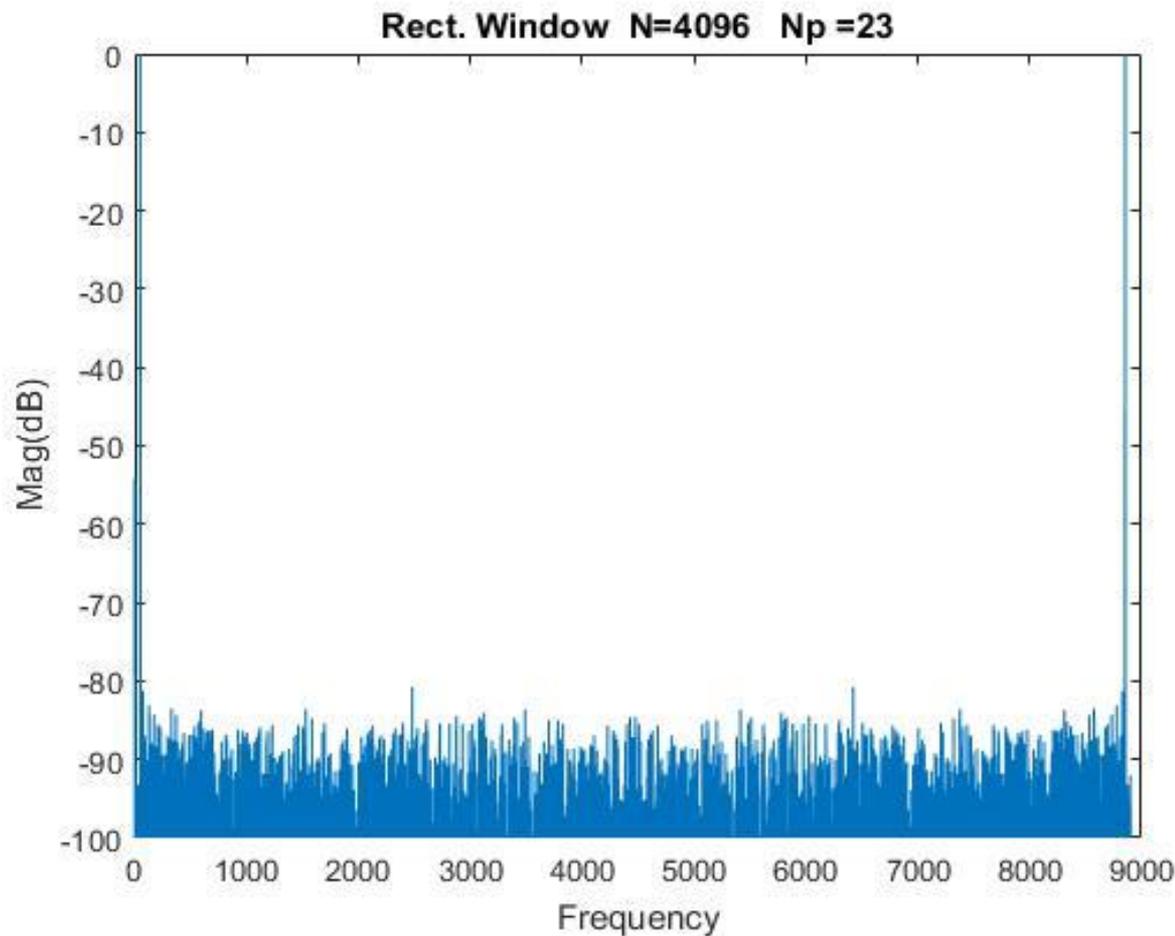
Quantization noise is much lower but still significant

Lets now increase oversampling ratio (i.e. number of samples)

Recall:

# Quantization Effects

Res = 10 bits



$f_{\text{SIG}}=50\text{Hz}$   
 $f_{\text{NYQ}}=100\text{Hz}$   
 $f_{\text{SAMP}}=8904\text{KHz}$   
Oversampled: 89:1

$$E_{\text{RMS}} = \frac{x_{\text{LSB}}}{\sqrt{12}}$$

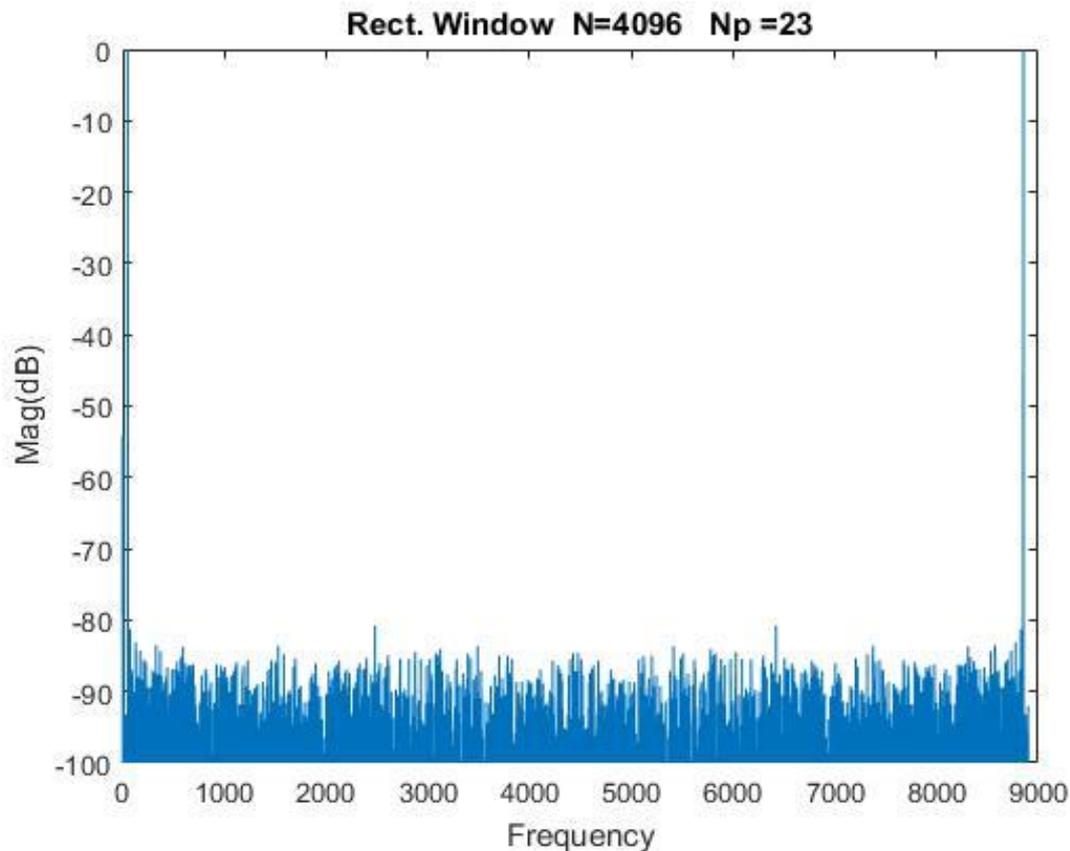
Compared to the previous slide, it appears that the quantization noise has gone down

But has it? Magnitude of quantization DFT terms decreased but  $E_{\text{RMS}}$  unchanged

Recall:

# Quantization Effects

Res = 10 bits



$$f_{\text{SIG}}=50\text{Hz}$$

$$f_{\text{NYQ}}=100\text{Hz}$$

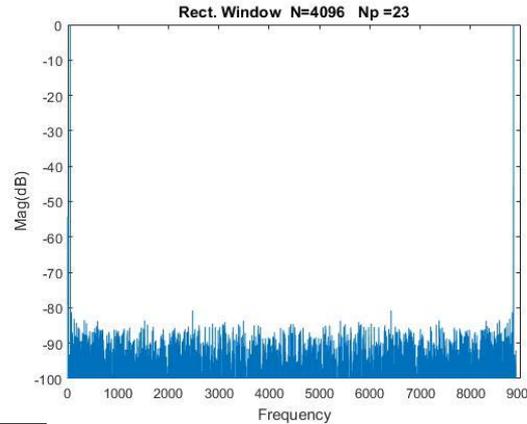
$$f_{\text{SAMP}}=8904\text{KHz}$$

Oversampled: 89:1

$$E_{\text{RMS}} = \frac{x_{\text{LSB}}}{\sqrt{12}}$$

Can any additional useful information about the input be obtained since we have many more samples than are needed?

# Over-Sampling



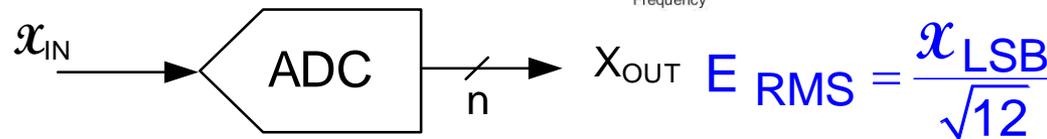
Res = 10 bits

$$f_{SIG} = 50\text{Hz}$$

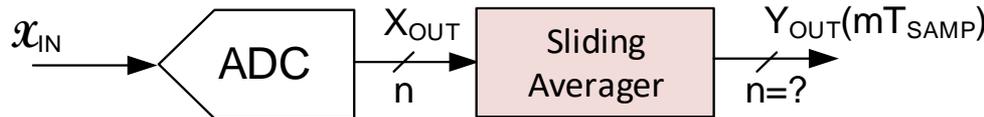
$$f_{NYQ} = 100\text{Hz}$$

$$f_{SAMP} = 8904\text{KHz}$$

Oversampled: 89:1



What happens if we break the 4096 samples into groups of 20 samples and form following?

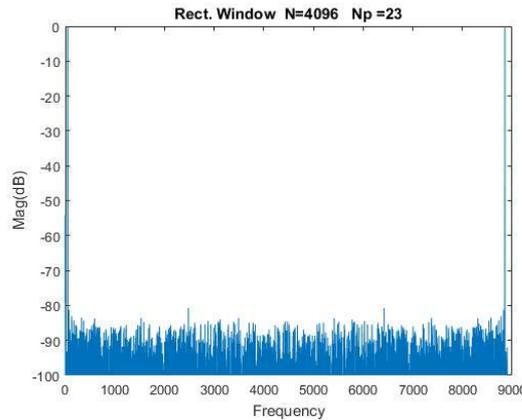


$$E_{RMS} = ?$$

$$Y_{OUT} = \hat{X}_{OUT}(k \cdot 20T_{SAMP}) = \frac{1}{20} \sum_{j=1}^{20} x_{OUT}(jT_{SAMP} + 20kT_{SAMP})$$

- Though the individual samples have been quantized to 10 bits, the arithmetic operations will have many more bits
- The effective sampling rate has been reduced by a factor of 20 but is still over 4 times the Nyquist rate
- Has the quantization noise been reduced (or equivalently has the resolution of the ADC been improved?)
- Is there more information available about the signal?

# Over-Sampling



Res = 10 bits

$$f_{\text{SIG}} = 50\text{Hz}$$

$$f_{\text{NYQ}} = 100\text{Hz}$$

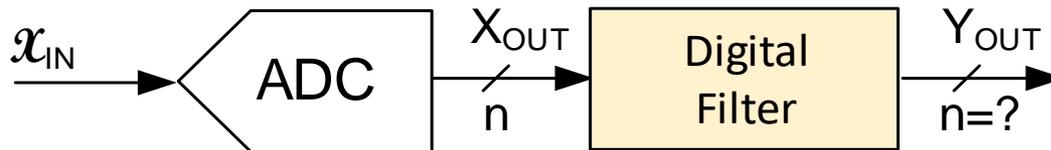
$$f_{\text{SAMP}} = 8904\text{KHz}$$

Oversampled: 89:1



$$E_{\text{RMS}} = \frac{x_{\text{LSB}}}{\sqrt{12}}$$

Since the quantization noise is at high frequencies, what would happen if filtered the Boolean output signal?



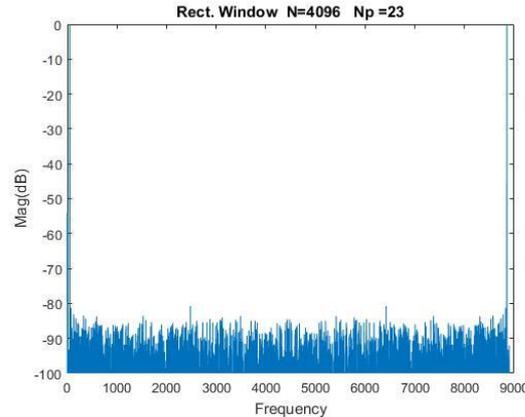
$$E_{\text{RMS}} = ?$$

$$Y_{\text{OUT}}(kT_{\text{SAMP}}) = \sum_{j=0}^m a_j x_{\text{OUT}}(k - jT_{\text{SAMP}})$$

Or

$$Y_{\text{OUT}}(kT_{\text{SAMP}}) = \sum_{j=0}^m a_j x_{\text{OUT}}(k - jT_{\text{SAMP}}) + \sum_{j=1}^h b_j Y_{\text{OUT}}(k - jT_{\text{SAMP}})$$

# Over-Sampling



Res = 10 bits

$f_{\text{SIG}}=50\text{Hz}$

$f_{\text{NYQ}}=100\text{Hz}$

$f_{\text{SAMP}}=8904\text{KHz}$

Oversampled: 89:1

What does this difference equation represent?

$$Y_{\text{OUT}}(kT_{\text{SAMP}}) = \sum_{j=0}^m a_j x_{\text{OUT}}(k - jT_{\text{SAMP}})$$

- Moving Average (MA) Digital Filter
- Filter shape (e.g. low-pass, band-pass, high-pass, ... dependent upon  $\langle a_i \rangle$  coefficients)

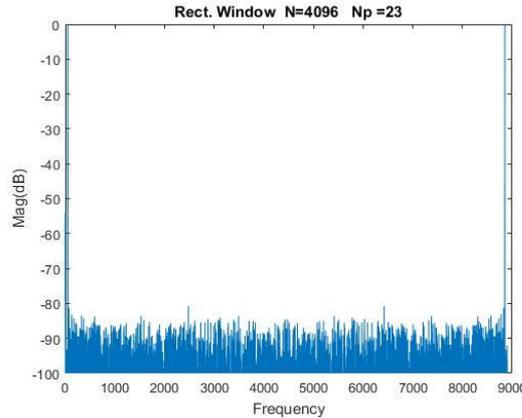
What does this difference equation represent?

$$Y_{\text{OUT}}(kT_{\text{SAMP}}) = \sum_{j=0}^m a_j x_{\text{OUT}}(k - jT_{\text{SAMP}}) + \sum_{j=1}^h b_j Y_{\text{OUT}}(k - jT_{\text{SAMP}})$$

- Auto Regressive Moving Average (ARMA) Digital Filter
- Filter shape (e.g. low-pass, band-pass, high-pass, ... dependent upon  $\langle a_i \rangle$  and  $\langle b_j \rangle$  coefficients)

$$E_{\text{RMS}} = \frac{x_{\text{LSB}}}{\sqrt{12}}$$

# Over-Sampling



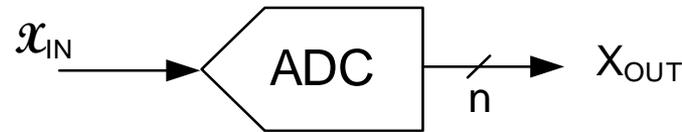
Res = 10 bits

$$f_{\text{SIG}} = 50\text{Hz}$$

$$f_{\text{NYQ}} = 100\text{Hz}$$

$$f_{\text{SAMP}} = 8904\text{KHz}$$

Oversampled: 89:1



$$E_{\text{RMS}} = \frac{x_{\text{LSB}}}{\sqrt{12}}$$

Since the quantization noise is at high frequencies, what would happen if we filtered and decimated the Boolean output signal?

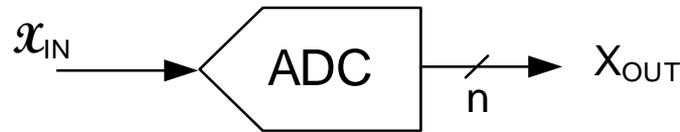
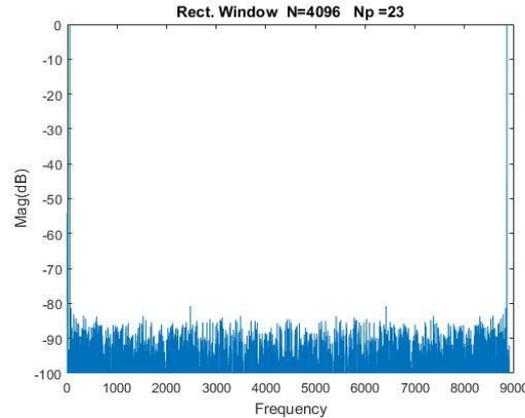
$$Y_{\text{OUT}}(kT_{\text{SAMP}}) = \sum_{j=0}^m a_j x_{\text{OUT}}(k - jT_{\text{SAMP}})$$

$$Y_{\text{OUT}}(kT_{\text{SAMP}}) = \sum_{j=0}^m a_j x_{\text{OUT}}(k - jT_{\text{SAMP}}) + \sum_{j=1}^h b_j Y_{\text{OUT}}(k - jT_{\text{SAMP}})$$

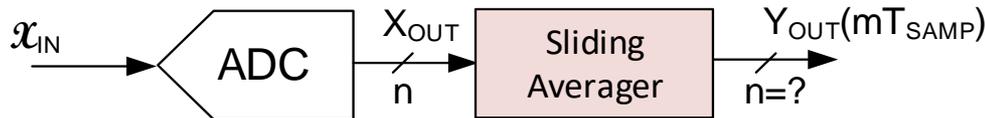


$$E_{\text{RMS}} = ?$$

# Over-Sampling



$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$



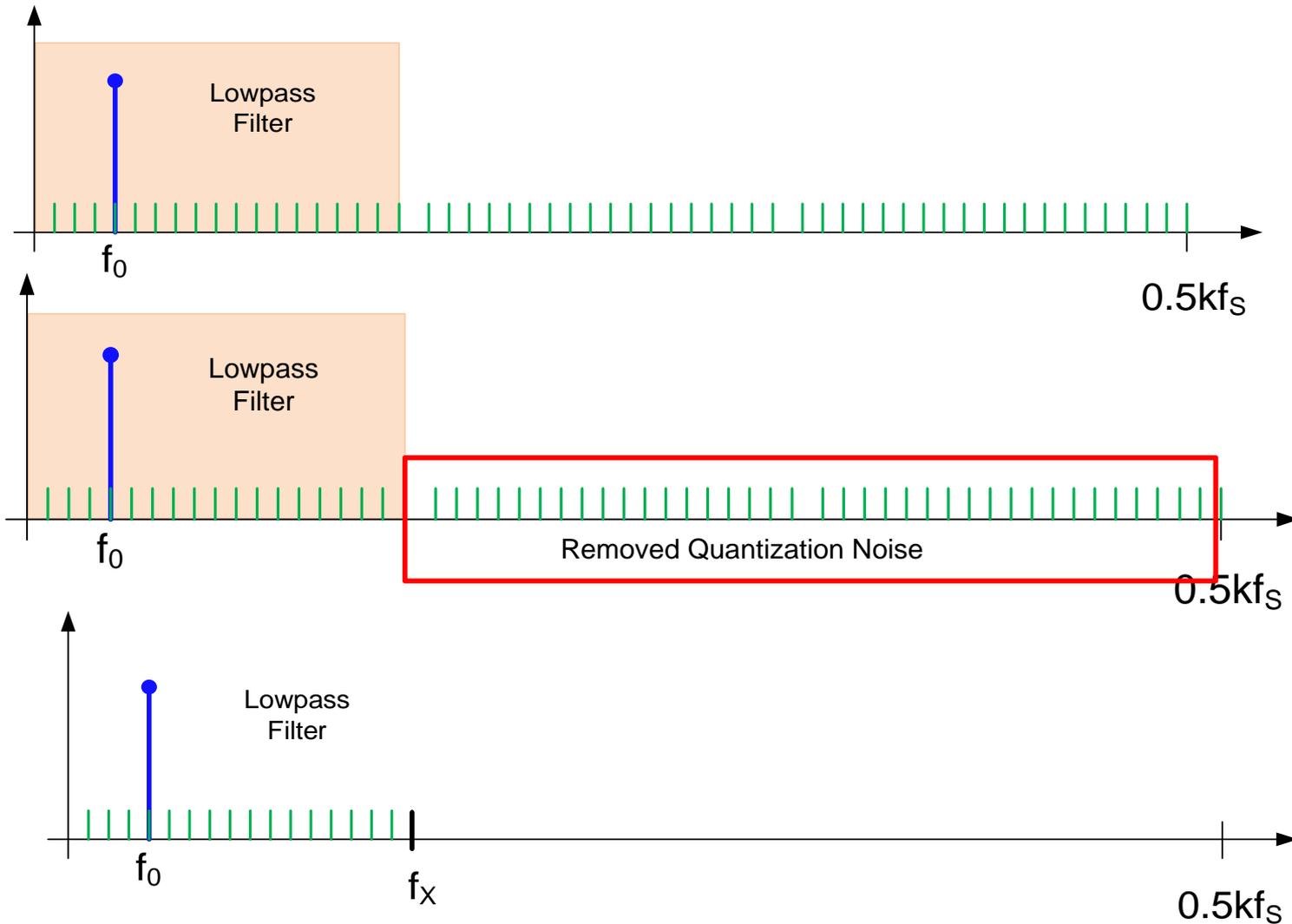
$$E_{RMS} = ?$$



$$E_{RMS} = ?$$

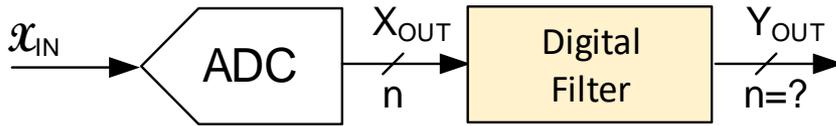
- What is the overhead?
- What is the performance potential?
- How can these or related over-sampling approaches be designed?
- Though this approach may help quantization noise, will not improve ADC linearity

# Over-Sampled Spectrum showing quantization noise with digital lowpass filter



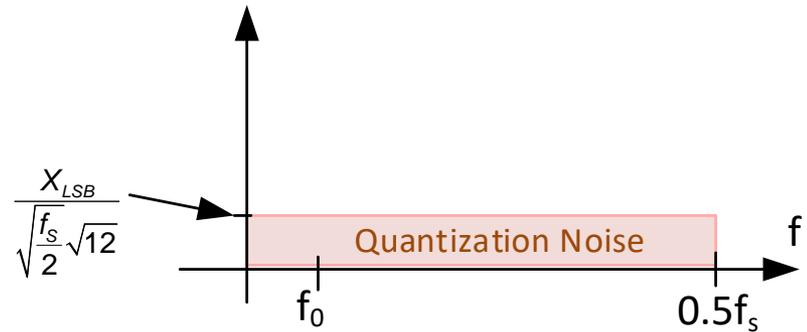
Residual Quantization Noise if Filter Band-edge at  $f_x$

# Over-Sampling



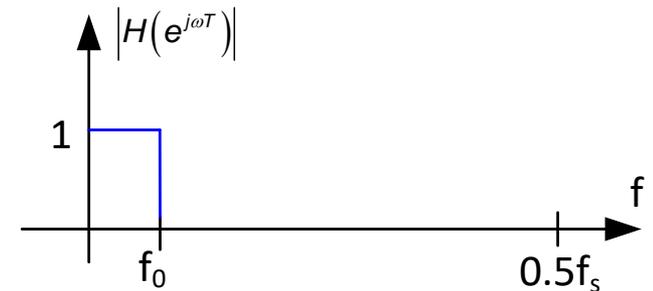
$$f_s = f_{\text{SAMP}}$$

$$OSR = \frac{f_s}{2 f_0}$$



With ideal lowpass filter with band-edge at  $f_0$

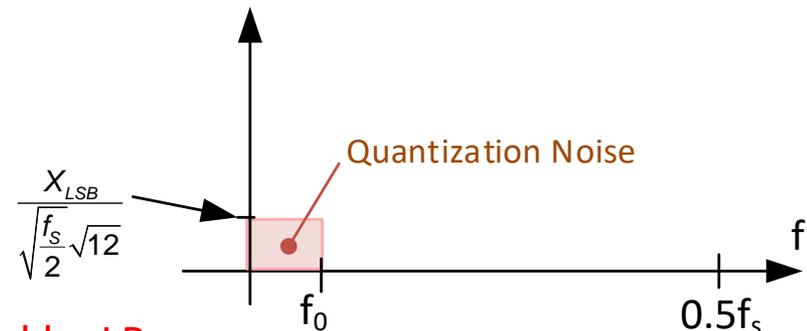
$$V_{Qrms} = \frac{V_{LSB}}{\sqrt{12}} \frac{1}{\sqrt{OSR}}$$



For sinusoidal input with p-p value  $V_{REF}$

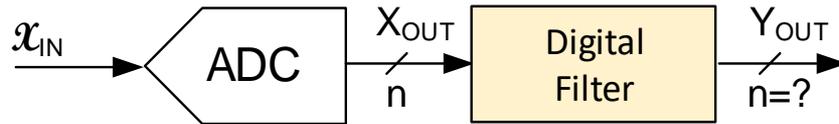
$$SNR = 6.02n + 1.76 + 10\log(OSR)$$

Improvement of 3dB/octave or 0.5bits/octave

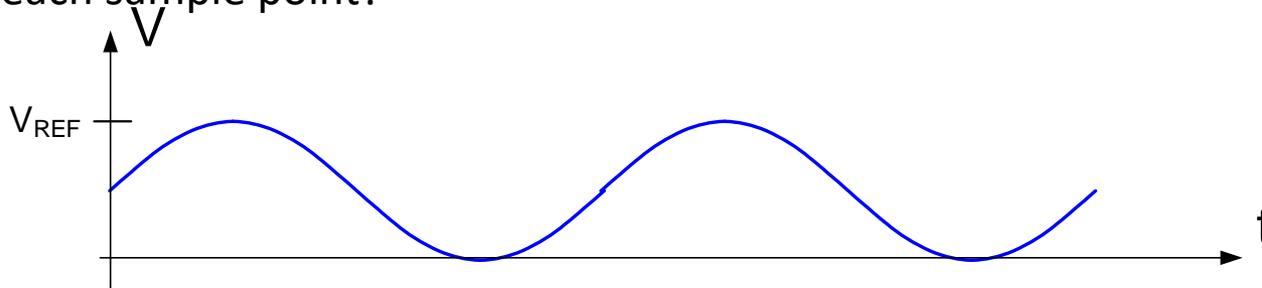


Oversampling increases resolution and if followed by LP filter Reduces Quantization Noise!

# Over-Sampling



Example: If we sample a sinusoidal waveform at a rate of 1000 samples/period with a 4-bit ADC and at each time we create a 16-point moving sum, how many digits will we have at each sample point?



What is the quantization noise of the 4-bit ADC?

$$V_{n\_RMS} = \frac{V_{LSB\_4}}{\sqrt{12}} = \frac{V_{REF}}{2^4 \sqrt{12}} = \frac{V_{REF}}{2^5 \sqrt{3}}$$

Have we created an 8-bit ADC by simply over sampling?

What is the quantization noise of the 8-bit ADC?

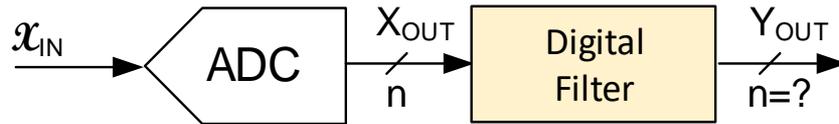
$$V_{n\_RMS} = \frac{V_{LSB\_8}}{\sqrt{12}} = \frac{V_{REF}}{2^8 \sqrt{12}} = \frac{V_{REF}}{2^9 \sqrt{3}}$$

If the 4-bit ADC has INL at the 16-bit level, what will be the INL of the 8-bit ADC?

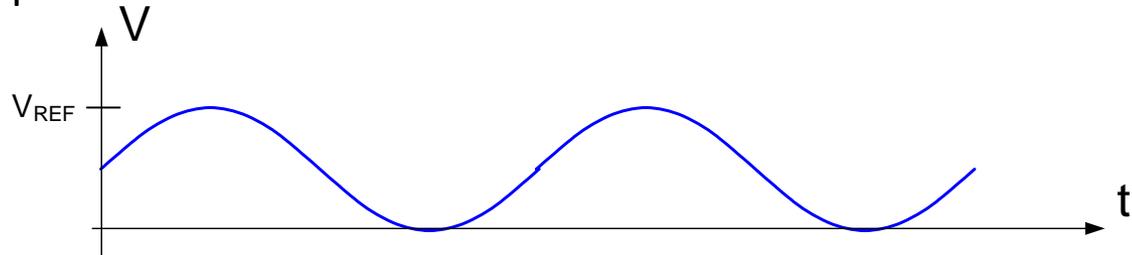
How many digital output codes will be present ?

256

# Over-Sampling



Example: If we sample a sinusoidal waveform at a rate of 1000 samples/period with a 4-bit ADC and at each time we create a 16-point moving sum, how many digits will we have at each sample point?



Have we created an 8-bit ADC by simply over sampling?

What is the quantization noise of the 8-bit ADC?

$$V_{n\_RMS} = \frac{V_{LSB\_8}}{\sqrt{12}} = \frac{V_{REF}}{2^8 \sqrt{12}} = \frac{V_{REF}}{2^9 \sqrt{3}}$$

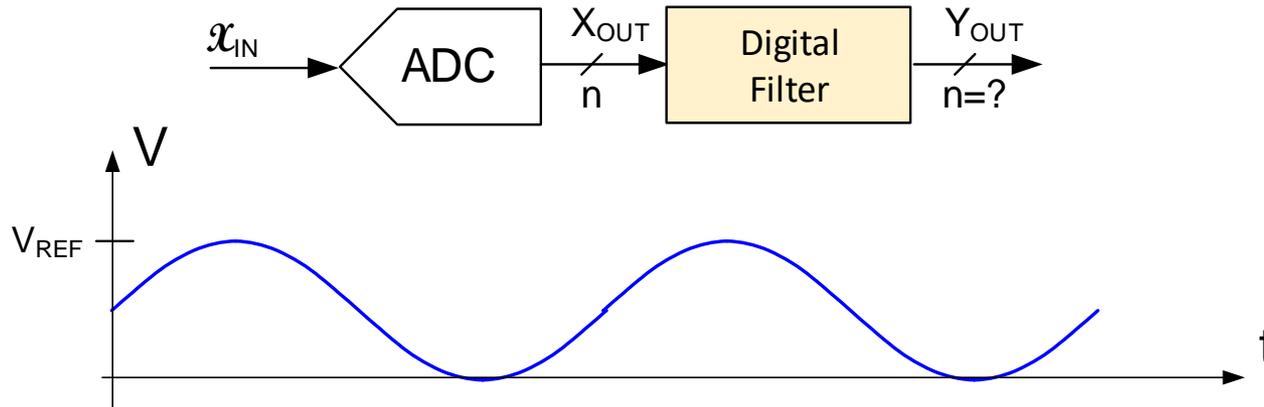
If the 4-bit ADC has INL at the 16-bit level, what will be the INL of the 8-bit ADC?      16-bit

How many digital output codes will be present ?      256

Is there much useful information in the many adjacent digital outputs?      No!

We can keep just one of every 16 outputs (termed decimation) without losing information about input - Thus effective throughput is reduced by factor of 16

# Over-Sampling



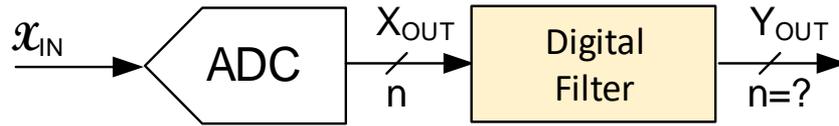
In the previous example, the Digital Filter was a MA filter, other Digital Filters could be used

Is over-sampling followed by digital filtering a practical way to increase the effective resolution of an ADC?

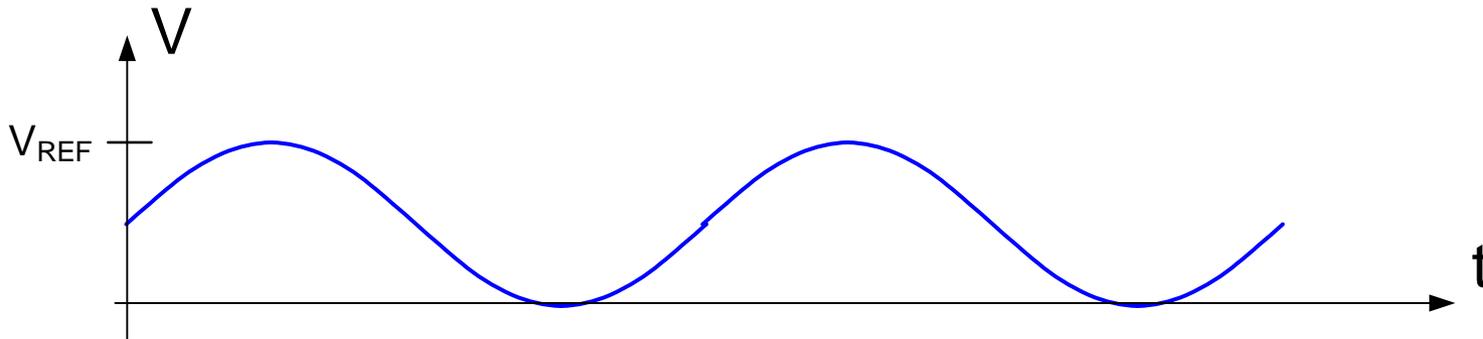
Is the digital computation overhead acceptable?

One limitation of this approach is that to get a major increase in effective resolution, the over sampling ratio gets very large since ENOB varies with the square root of the OSR

# Over-Sampling



Consider same 4-bit ADC with 16-point Moving Average digital filter



What will be the output if a constant input is applied ?

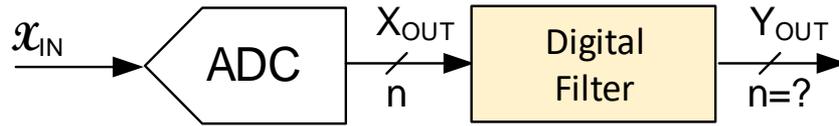


Will it still be an 8-bit output?

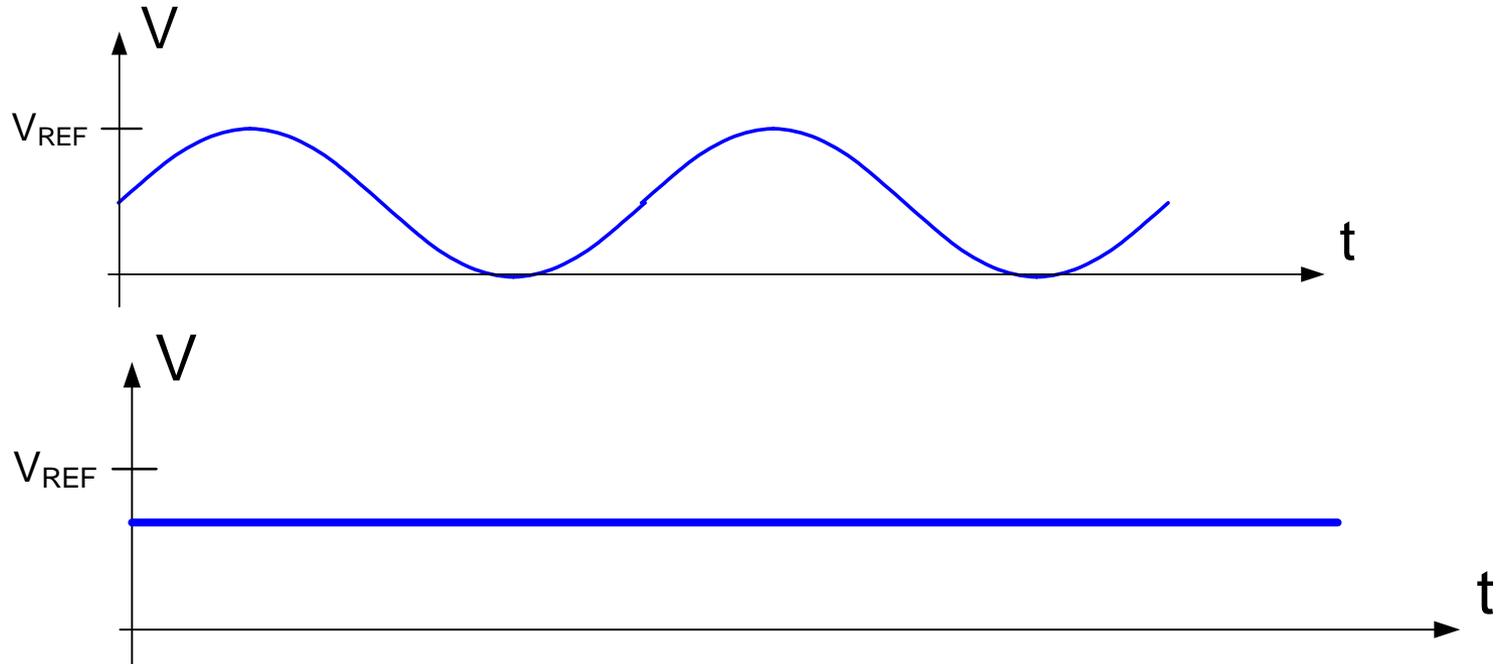
If a large number of constant input signals are applied, how many output codes will there be?

16

# Over-Sampling



Consider same 4-bit ADC with 16-point Moving Average digital filter

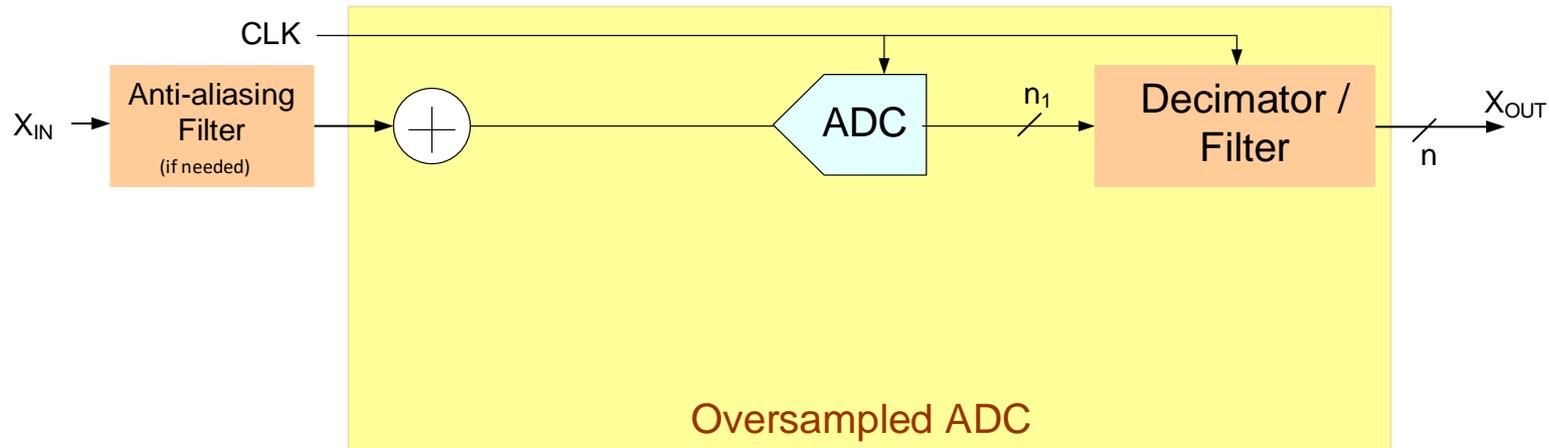


Be careful about performance relative to speckmanship !

Is there some way to actually take advantage of the over-sampling to increase the apparent resolution without facing the static resolution problem?

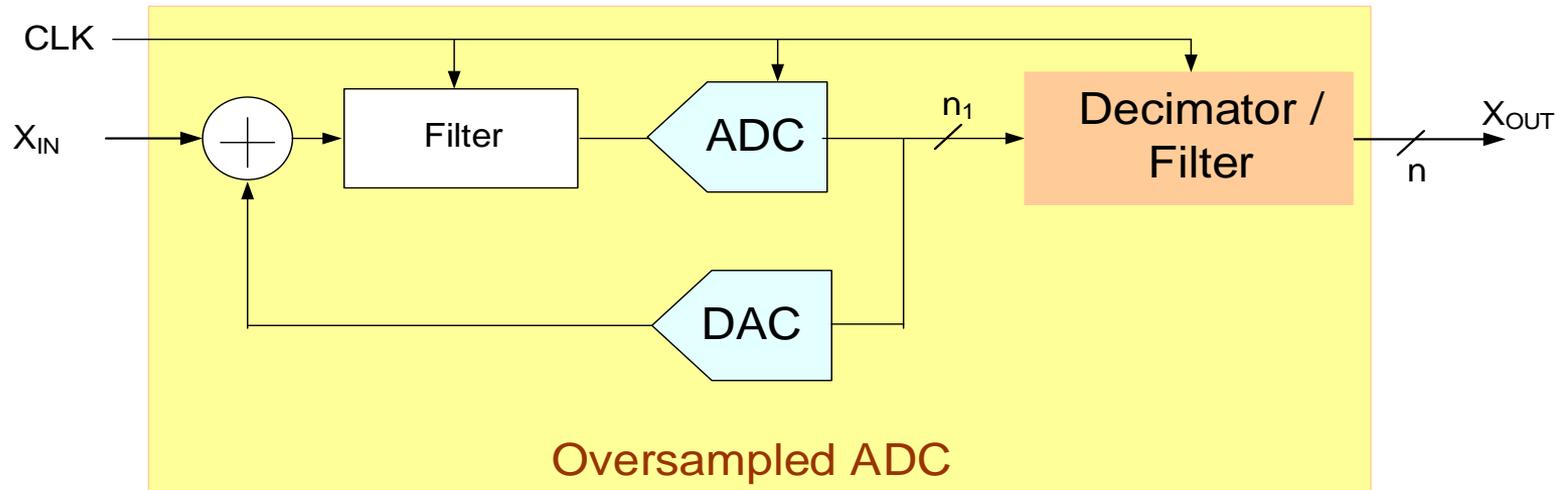
Can add random noise, or dither, or use  $\Delta\Sigma$  modulation or other ways as well

# Over-sampled ADC



- Anti-aliasing filter at the input (if needed) to limit bandwidth of input signal
- ADC is often simply a comparator
- CLK is much higher in frequency than effective sampling rate (maybe 128:1 though lower OSR also widely used)
- Can obtain very high resolution but effective sampling rate is small
- **With clever design, this approach can reduce quantization effects and improve linearity (but the oversampling does not improve linearity)**
- **A modulator can be added along with oversampling to reduce OS overhead to form Delta-Sigma ADC**

# Over-sampled $\Delta\Sigma$ ADC (Delta-Sigma)



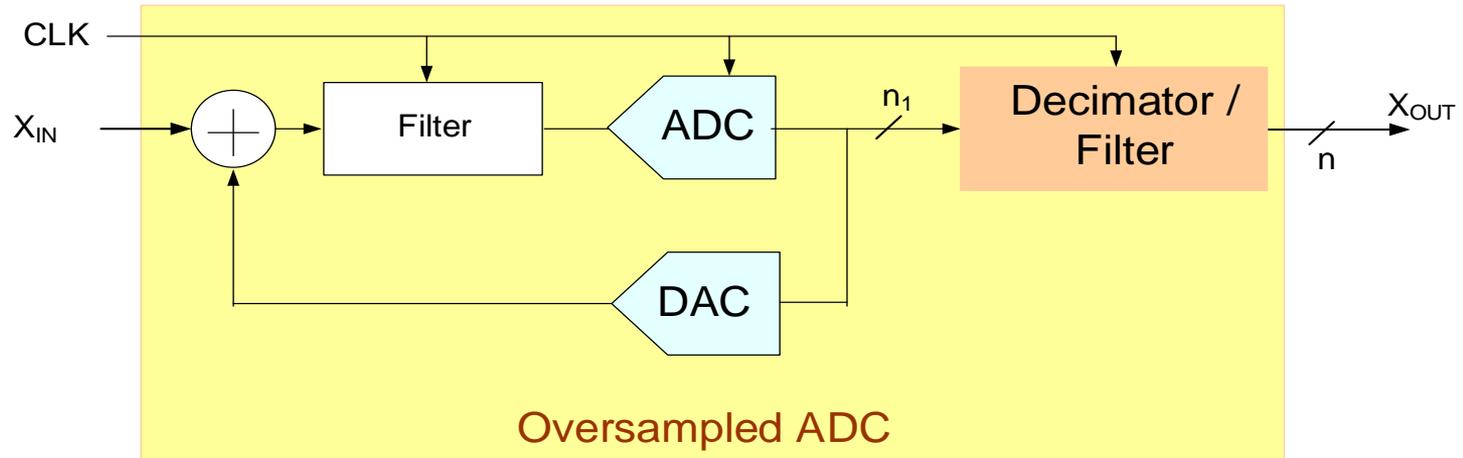
If Modulator is added, the over-sampled ADC becomes a  $\Delta\Sigma$  ADC

$\Delta$  modulation introduced by Deloraine in 1946

$\Delta\Sigma$  ADC concept introduced by Yasuhiko Yasuda in the early 1960's while he was a student at [the University of Tokyo](#)

Candy (1974) and Temes credited with incorporating the concept in integrated data converters

# Over-sampled $\Delta\Sigma$ ADC (Delta-Sigma)

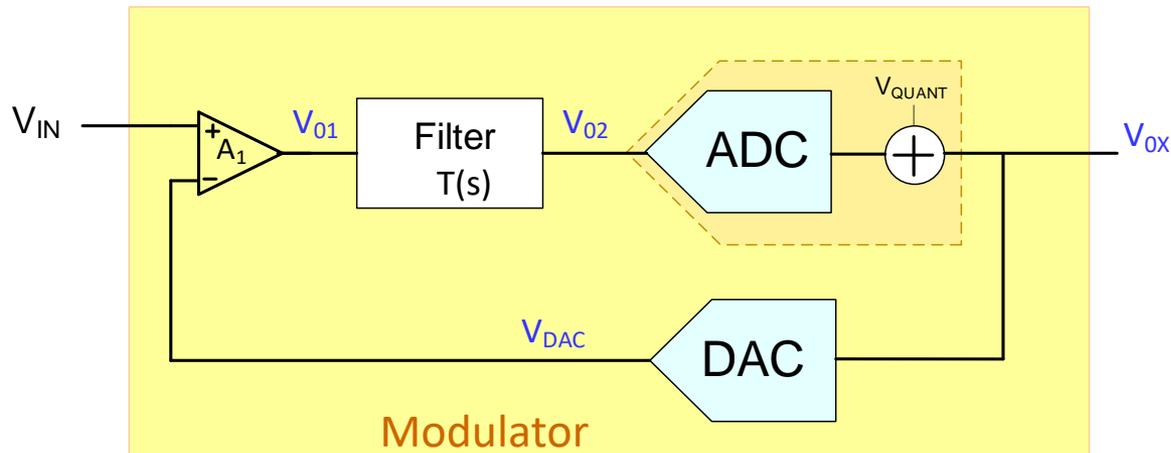


- Linearity performance almost entirely determined by that of the DAC (key property – can think of ADC “guessing” at what input is)
- 1-bit DAC (i.e. only a comparator for ADC) is inherently linear and widely used
- 20-bit linearity is achievable without any trimming using 1-bit DAC
- The modulator provides what is termed “noise shaping”

Comment: To obtain 16-bit linearity with a 10-bit DAC, the 10-bit DAC must be linear to at least the 16-bit level. This would usually require tedious trimming of the DAC

# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)



Assume gain of ADC and DAC are 1

$$V_{O1} = A_1 (V_{IN} - V_{DAC})$$

$$V_{O2} = T(s) V_{O1}$$

$$V_{OX} = V_{O2} + V_{QUANT}$$

$$V_{DAC} = V_{OX}$$

Solving, we obtain

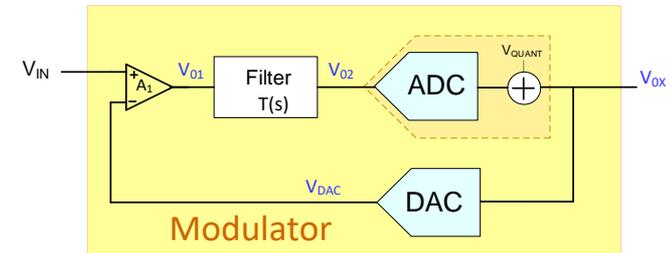
$$V_{OX} = \frac{T(s)A_1}{1 + T(s)A_1} V_{IN} + V_{QUANT} \frac{1}{1 + T(s)A_1}$$

Note: Significantly different transfer functions for  $V_{IN}$  and  $V_{QUANT}$

# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

$$V_{OX} = \frac{T(s)A_1}{1+T(s)A_1} V_{IN} + V_{QUANT} \frac{1}{1+T(s)A_1}$$



Consider using an integrator for  $T(s)$

$$T(s) = \frac{I_{01}}{s}$$

$I_{01}$  is the unity gain frequency of the integrator and is a critical parameter in the modulator

Thus

$$V_{OX} = \frac{I_{01}A_1}{s + I_{01}A_1} V_{IN} + V_{QUANT} \frac{s}{s + I_{01}A_1}$$

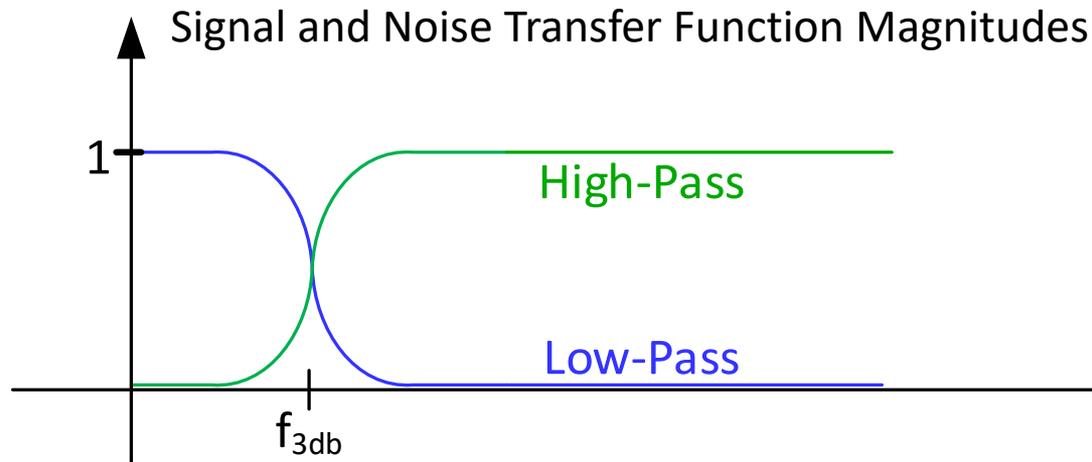
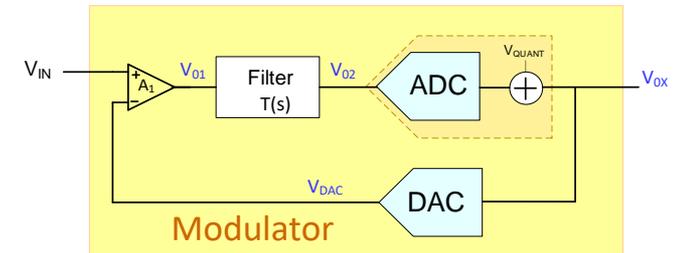
Note  $V_{IN}$  is low-pass filtered and  $V_{QUANT}$  is high-pass filtered and both are first-order with the same poles

# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

$$V_{OX} = \frac{I_{01}A_1}{s + I_{01}A_1} V_{IN} + V_{QUANT} \frac{s}{s + I_{01}A_1}$$

With integrator for  $T(s)$

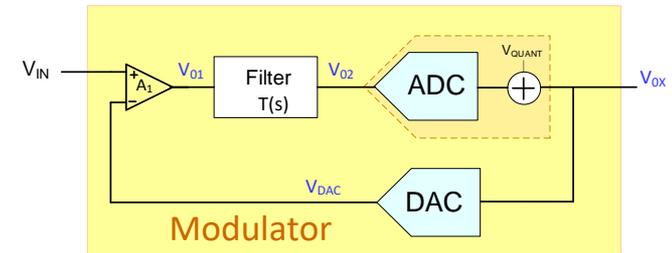


- Noise filtering will remove most of the noise from the signal band if the pole placed around signal band edge
- Signal band will not be significantly affected
- Filtering the noise is termed “noise shaping” in the vernacular of the delta-sigma community
- Since gain is 1 at high frequencies, HP filter does not increase spectral magnitude of noise at high frequencies

# Analysis of Delta-Sigma ADC

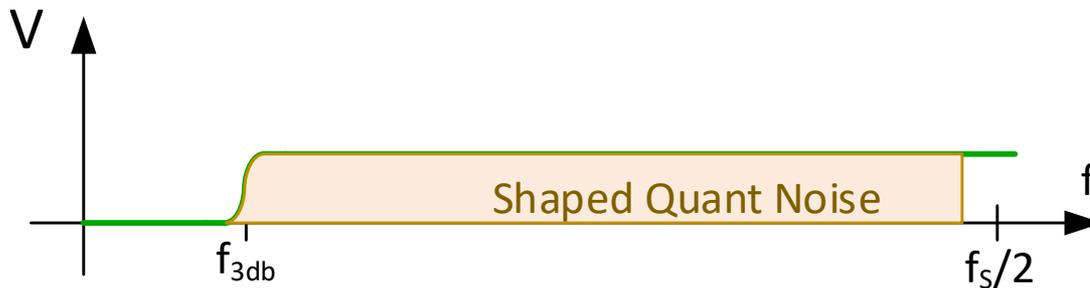
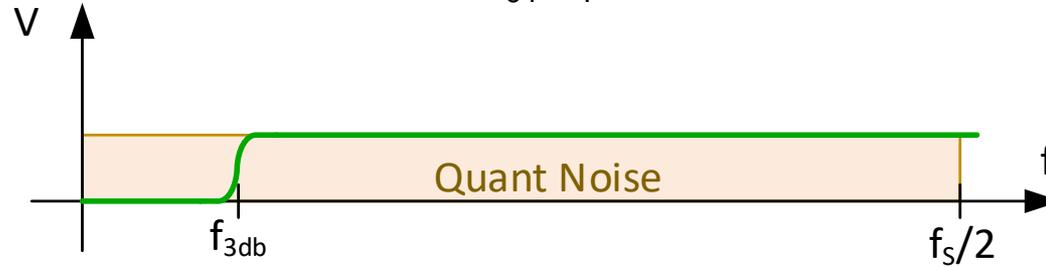
(big benefit is noise shaping)

$$V_{OX} = \frac{I_{01}A_1}{s + I_{01}A_1} V_{IN} + V_{QUANT} \frac{s}{s + I_{01}A_1}$$



Consider the noise output first

$$V_{OX-noise} = V_{QUANT} \frac{s}{s + I_{01}A_1} \quad f_{3dB} = I_{01}A_1$$

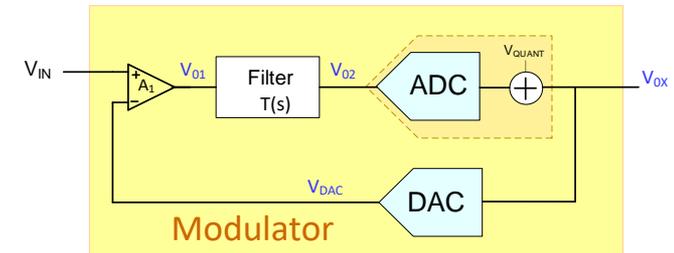


Major change in quantization noise spectral density at output

# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

$$V_{OX} = \frac{I_{01}A_1}{s + I_{01}A_1} V_{IN} + V_{QUANT} \frac{s}{s + I_{01}A_1}$$



Consider the input signal

$$V_{OX-IN} = V_{IN} \frac{I_{01}A_1}{s + I_{01}A_1}$$

$$f_{3dB} = I_{01}A_1$$

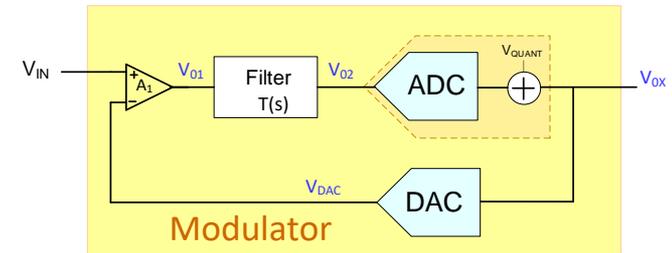


Little change in spectrum of input at the output

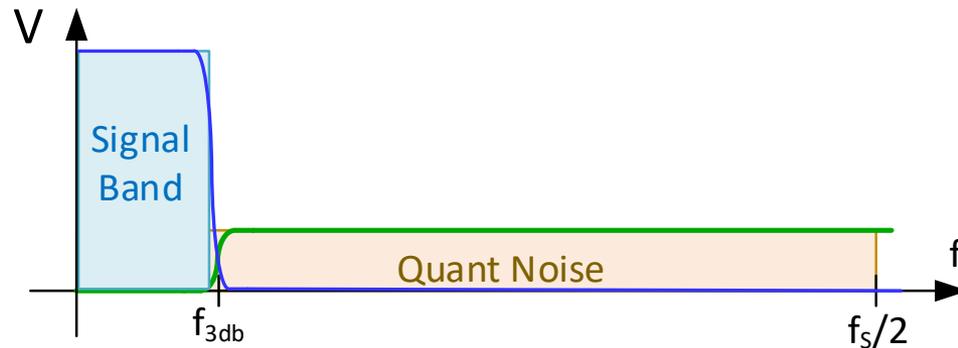
# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

$$V_{OX} = \frac{I_{01}A_1}{s + I_{01}A_1} V_{IN} + V_{QUANT} \frac{s}{s + I_{01}A_1}$$



Combined effects



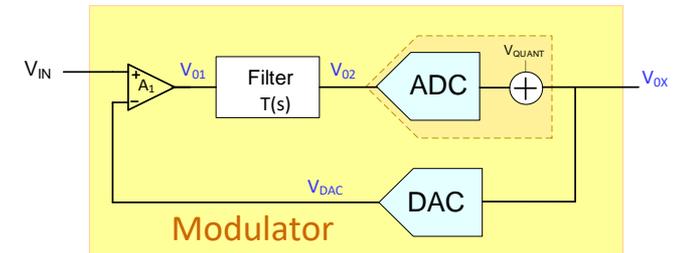
Remaining quantization noise can be dramatically reduced by a low-pass digital filter following modulator with band-edge around  $f_{3dB}$

The low-pass digital filter would have little effect on the signal band

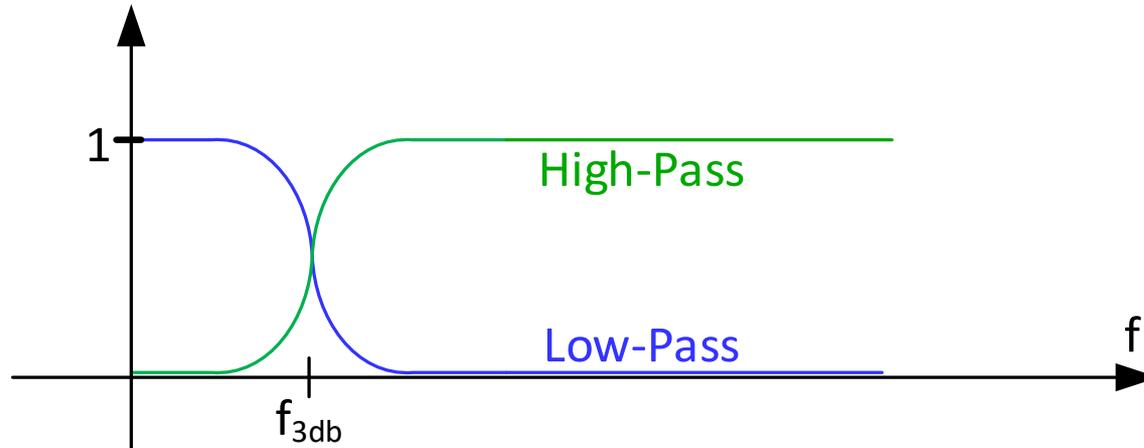
# Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

$$V_{OX} = \frac{T(s)A_1}{1+T(s)A_1} V_{IN} + V_{QUANT} \frac{1}{1+T(s)A_1}$$



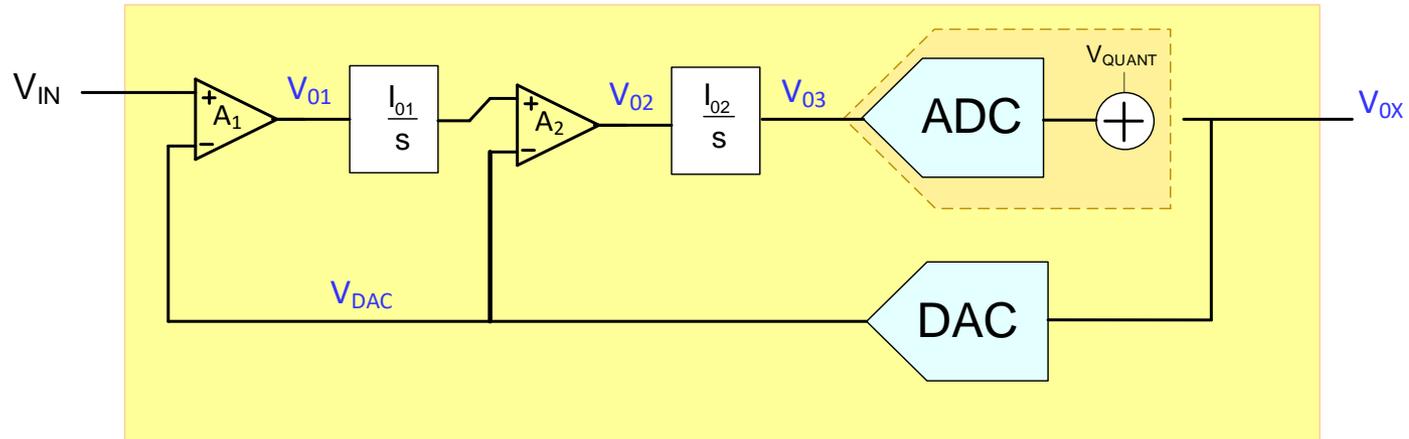
Signal and Noise Transfer Function Magnitudes



- A more selective filter (of higher order) would shape the noise even more and affect the passband even less if band edges are coincident
- Ideal low-pass and high-pass filters with coincident band edges followed by digital filter at output would allow nearly complete removal of the quantization noise !!

# Second-order Delta-Sigma ADC

(big benefit is noise shaping)



Modulator only shown with two integrators

$$V_{01} = A_1 (V_{IN} - V_{DAC})$$

$$V_{02} = A_2 \left[ \frac{I_{01}}{s} V_{01} - V_{DAC} \right]$$

$$V_{03} = \frac{I_{02}}{s} V_{02}$$

$$V_{OX} = V_{03} + V_{QUANT}$$

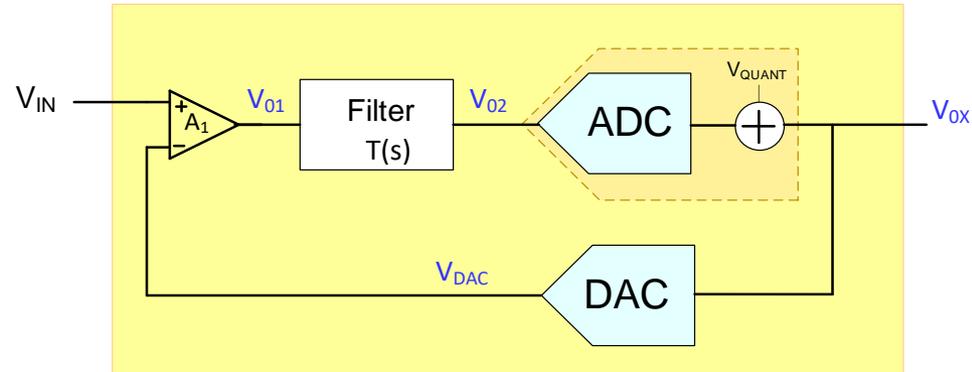
$$V_{DAC} = V_{OX}$$

Solving, obtain

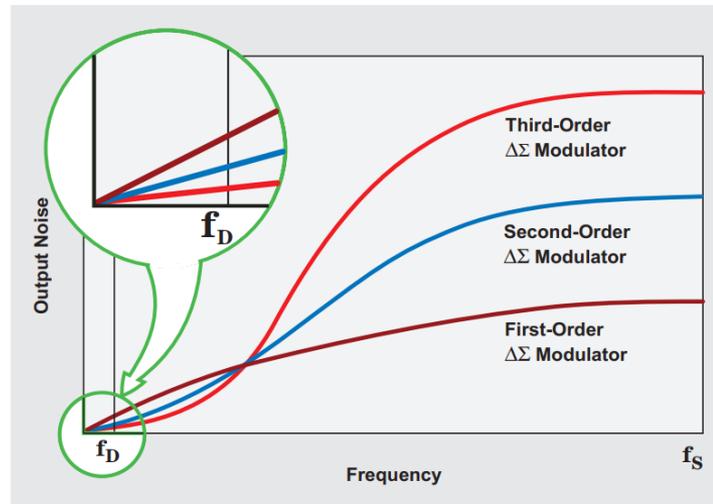
$$V_{OX} = \frac{I_{01} I_{02} A_1 A_2}{s^2 + s I_{02} A_2 + I_{01} I_{02} A_1 A_2} V_{IN} + \frac{s^2}{s^2 + s I_{02} A_2 + I_{01} I_{02} A_1 A_2} V_{QUANT}$$

# Higher-order Delta-Sigma ADC

(big benefit is noise shaping)



Much sharper transition between noise pass-band and signal stop band



From SLYT423 by Texas Instruments (author Bonnie Baker)

Baker reported TI used up to 6<sup>th</sup> order filters in SLYT423

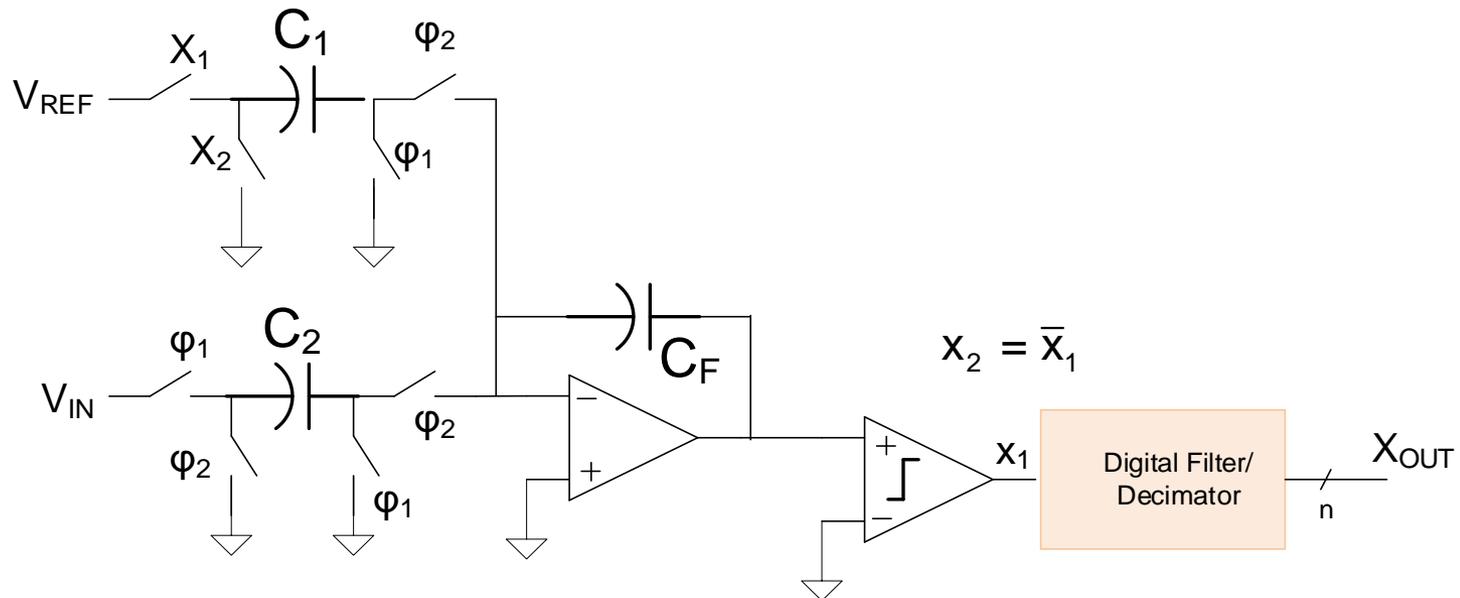
# First-Order Delta-Sigma ADC

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—1: FUNDAMENTAL THEORY AND APPLICATIONS, VOL. 50, NO. 3, 8

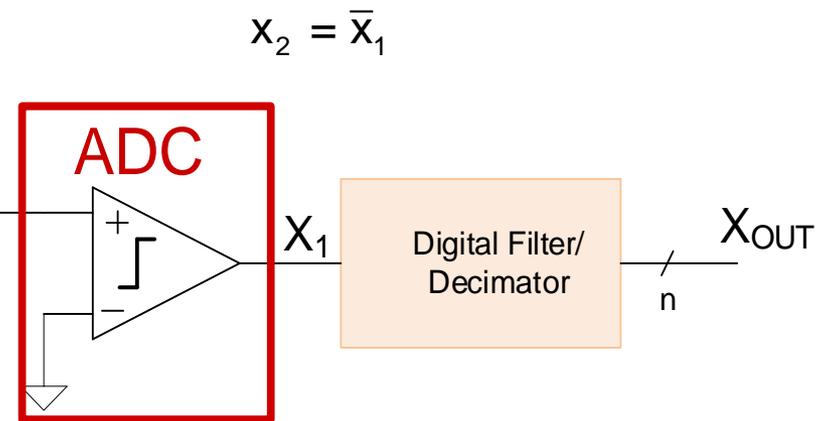
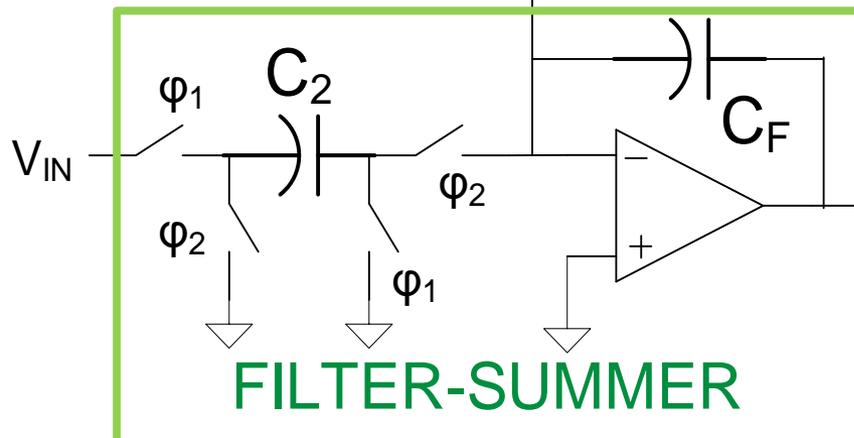
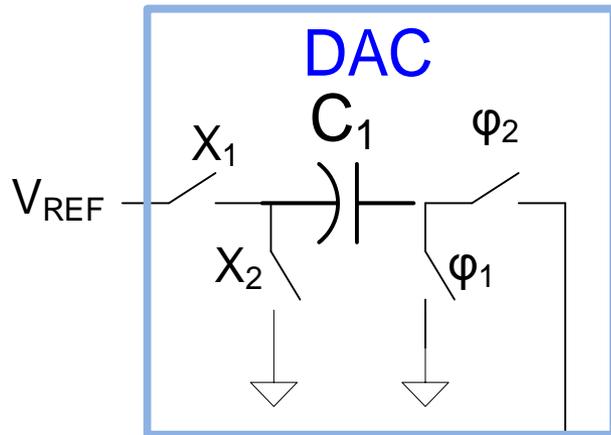
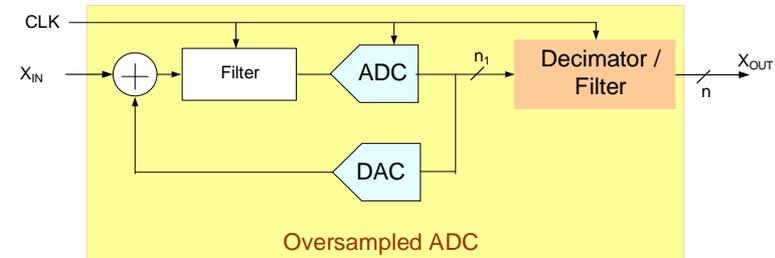
## Behavioral Modeling of Switched-Capacitor Sigma-Delta Modulators

Piero Malcovati, *Member, IEEE*, Simona Brigati, *Member, IEEE*, Fabrizio Francesconi, *Member, IEEE*, Franco Maloberti, *Fellow, IEEE*, Paolo Cusinato, and Andrea Baschirotto, *Senior Member, IEEE*

SC Circuits often used for Modulator



# First-Order Delta-Sigma ADC



# Over-sampled $\Delta\Sigma$ ADC)

Oversampling Alone:

$$SNR = 6.02n + 1.76 + 10\log(OSR)$$

0.5 bits/octave

Oversampling and First-Order Modulator:

$$SNR = 6.02n + 1.76 - 5.17 + 30\log(OSR)$$

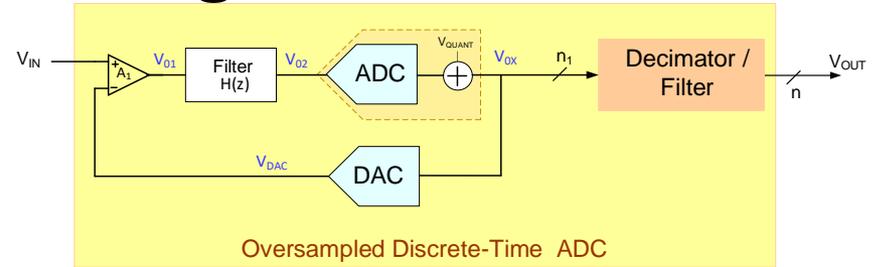
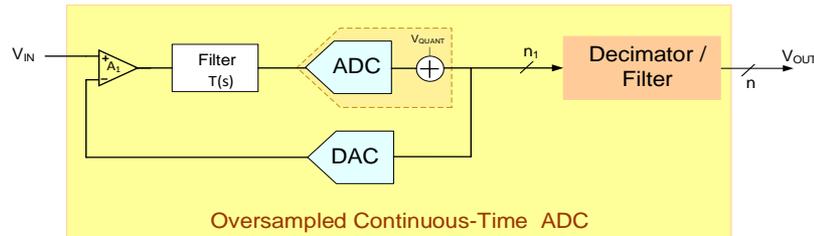
1.5 bits/octave

Oversampling and Second-Order Modulator:

$$SNR = 6.02n + 1.76 - 12.9 + 50\log(OSR)$$

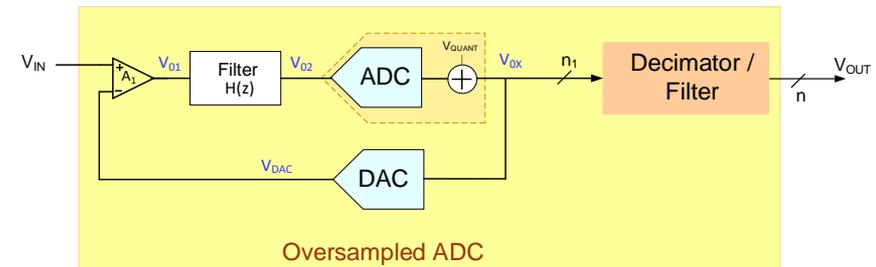
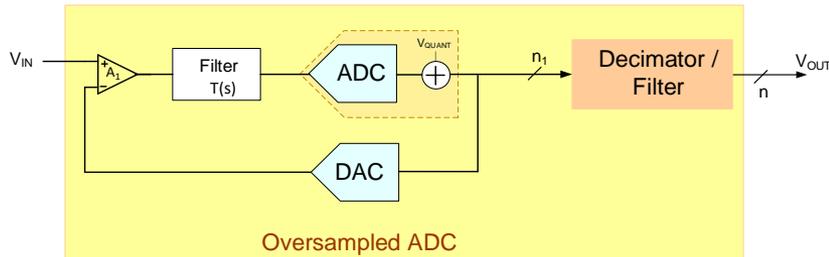
2.5 bits/octave

# Continuous-Time (CT) vs Discrete-Time (DT) Over-sampled Delta-Sigma ADCs



1. Input sampling errors for DT structures are never recovered
2. Nonlinearity of switches of concern in DT structures
3. No good switched in bipolar processes
4. Clock jitter adversely affects performance of discrete-time structures
5. Slew-rate requirements higher for DT structures and signal swings generally higher too
6. DT structures need additional headroom for switch control
7. CT structures can operate at lower supply voltages and lower power levels
8. Linearity of filter of increased concern in CT structures (particularly when using gm-C filters)
9. Transient response of DAC of increased concern in CT structures

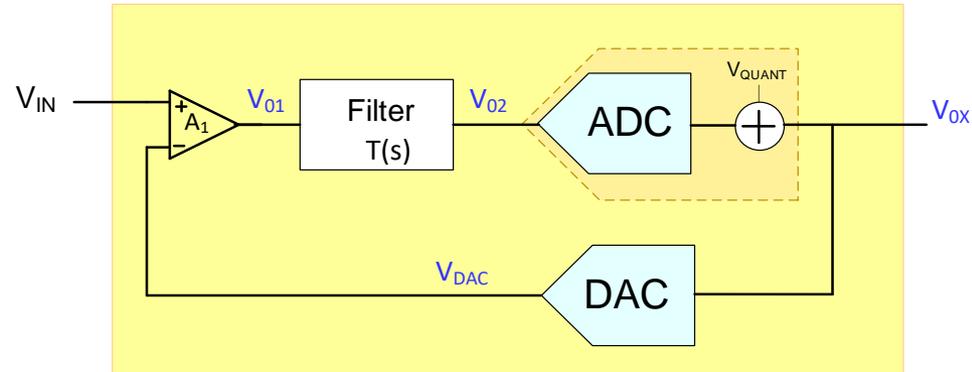
# Peculiar Issues with Over-sampled Delta-Sigma ADCs



1. Increasing resolution of DAC, OSR, and filter order (in the right way) all offer potential for increasing ENOB
2. Output is not completely repeatable for a given input
3. Some dc inputs will introduce idle tones or spectral lines in the output
4. Dynamic range requirements for both the filter and the ADC may be high to avoid saturation
5. Stability analysis may be challenging and require extensive time-domain simulations (because of nonlinearities, analytically not practical)
6. OSDS-ADCs are insensitive to errors in ADC though ADC errors may increase the amount of over-range required for filter
7. Although nonlinearity in the signal-band of the filter is important, it is usually not difficult to obtain
8. Nonlinearity errors of the DAC directly introduce nonlinearity in the OSDS-ADC so excellent DAC linearity is generally required
9. Dead zones (input regions with no output) may exist

# Higher-order Delta-Sigma ADC

(big benefit is noise shaping)



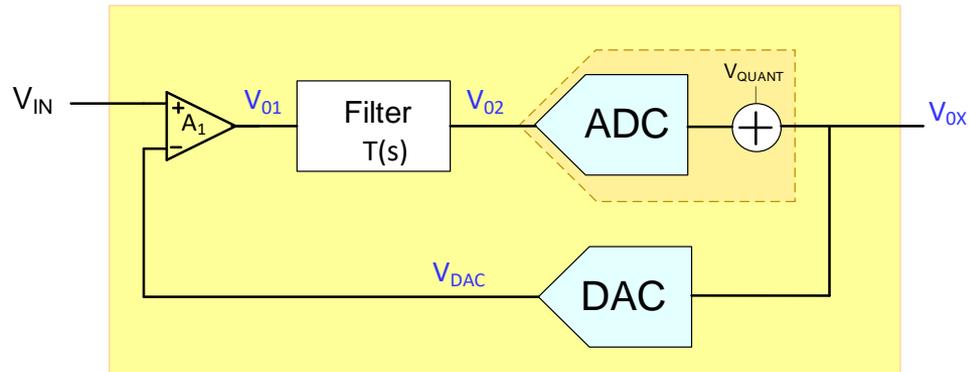
Excellent Material on Delta-Sigma ADCs

“How delta-sigma ADCs work ( Part 1 and Part 2)”

Author: Bonnie Baker

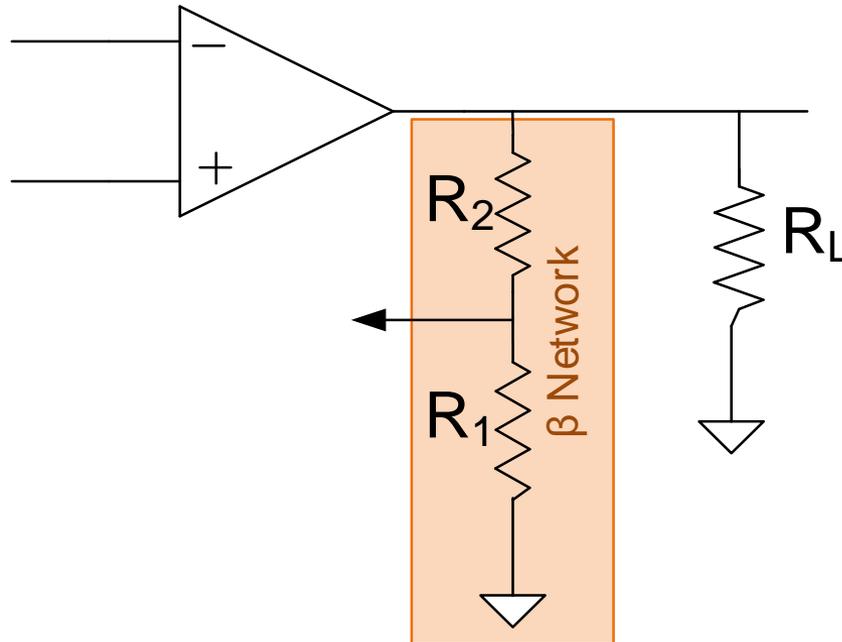
SLYT423 Revised Sept 2016 by Texas Instruments

# Delta-Sigma ADC Summary



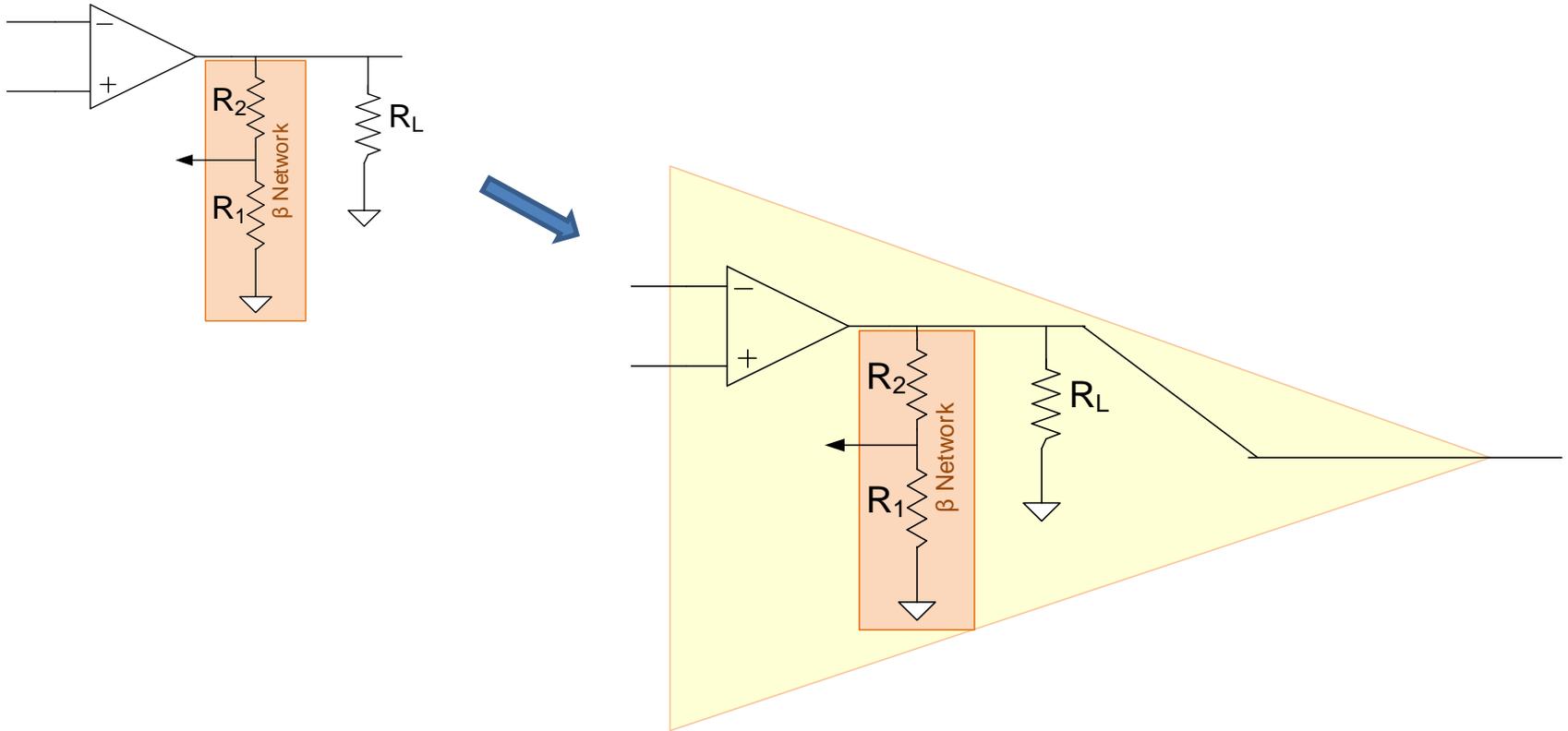
- **Key Goal of Delta Sigma ADC is to Reduce Quantization Noise**
  - Uses oversampling and noise shaping to achieve this
  - Effects can be dramatic (over 20-bit performance practical)
  - Circuits can be simple
  - Architecture of choice for high resolution INL-based ENOB applications
- **Delta Sigma ADC Does Nothing to Improve Linearity**
  - But first-order  $\Delta$ - $\Sigma$  ADC is inherently linear
  - Performance of DAC is critical, other components relaxed
- **Matching Requirements often Less Challenging**
  - No matching required for first-order  $\Delta$ - $\Sigma$
  - Order of DAC usually much less than that of  $\Delta$ - $\Sigma$
- **Speed of Delta-Sigma ADC Inherently Low**
  - But still high enough to be useful in many applications

# Output Stages



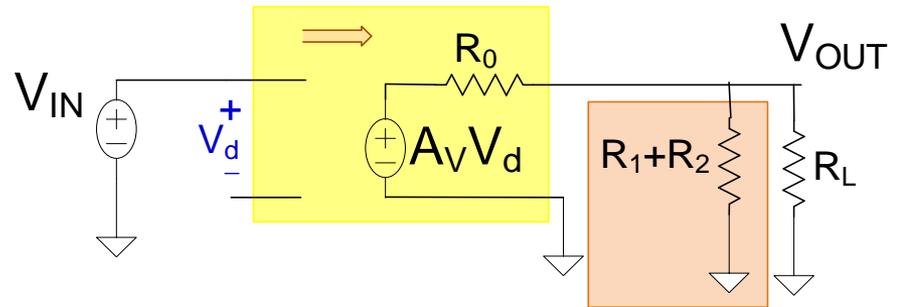
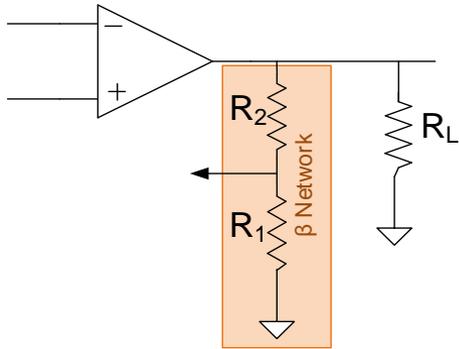
- Resistive Loading of Op Amp by  $R_L$  or  $\beta$  network reduces effective open loop gain
- Gain for most op amp architectures is increased by increasing output impedance
- Effective gain reduction can be dramatic

# Output Stages



Approximate Equivalent Open-Loop Amp

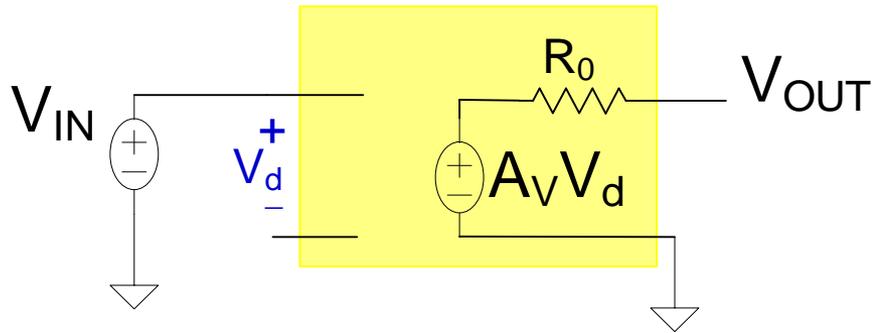
# Output Stages



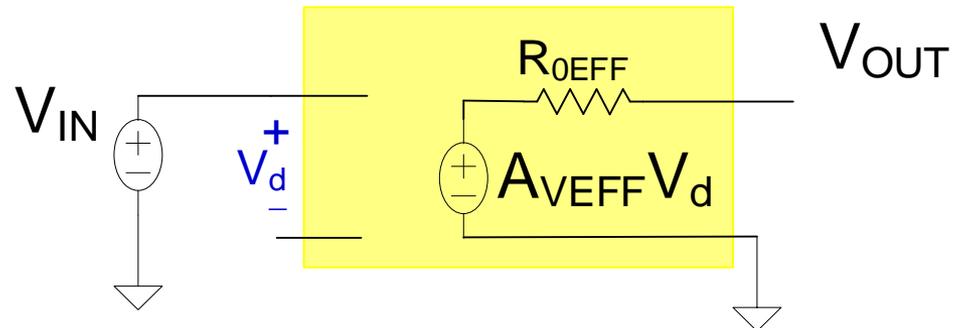
$$A_{VEFF} = A_V \frac{R_L // (R_1 + R_2)}{R_0 + R_L // (R_1 + R_2)}$$

$$R_{OEFF} = R_0 // R_L // (R_1 + R_2)$$

# Output Stages



Approximate Equivalent Open-Loop Amp  
Includes Resistive Loading of Load and  $\beta$  Network

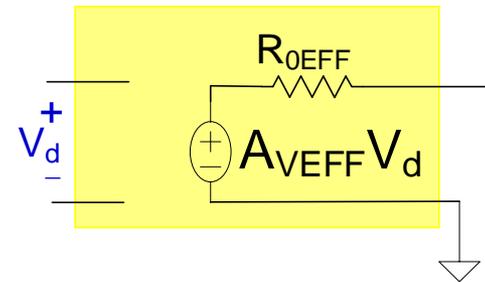
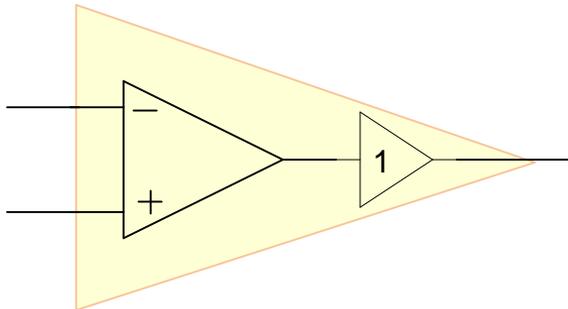
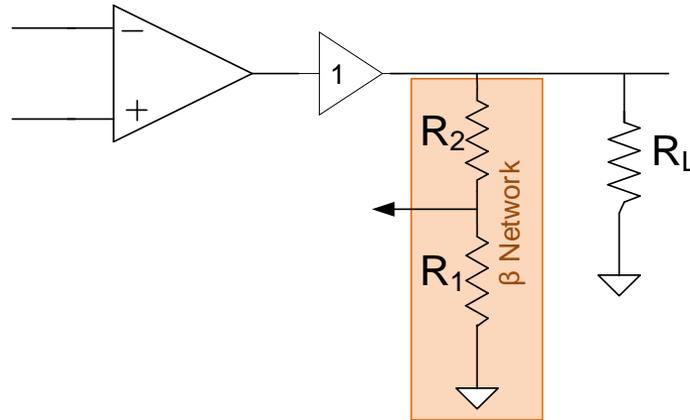


$$A_{VEFF} = A_V \frac{R_L // (R_1 + R_2)}{R_0 + R_L // (R_1 + R_2)}$$

$$R_{0EFF} = R_0 // R_L // (R_1 + R_2)$$

# Output Stages

Conceptual Solution to Resistive Loading Problem:  
 Add Buffer between Op Amp and Resistive Load



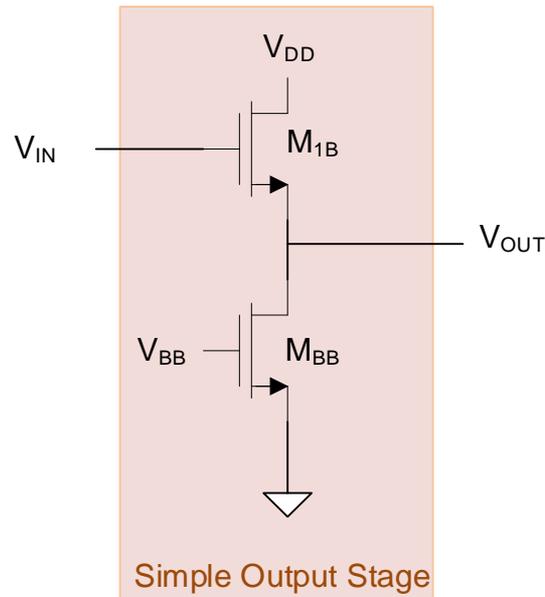
Approximate Equivalent Open-Loop Amp

$$A_{VEFF} = A_V$$

$$R_{OEFF} = R_{O-Buffer} \approx 0\Omega$$

**Buffer Termed Output Stage**

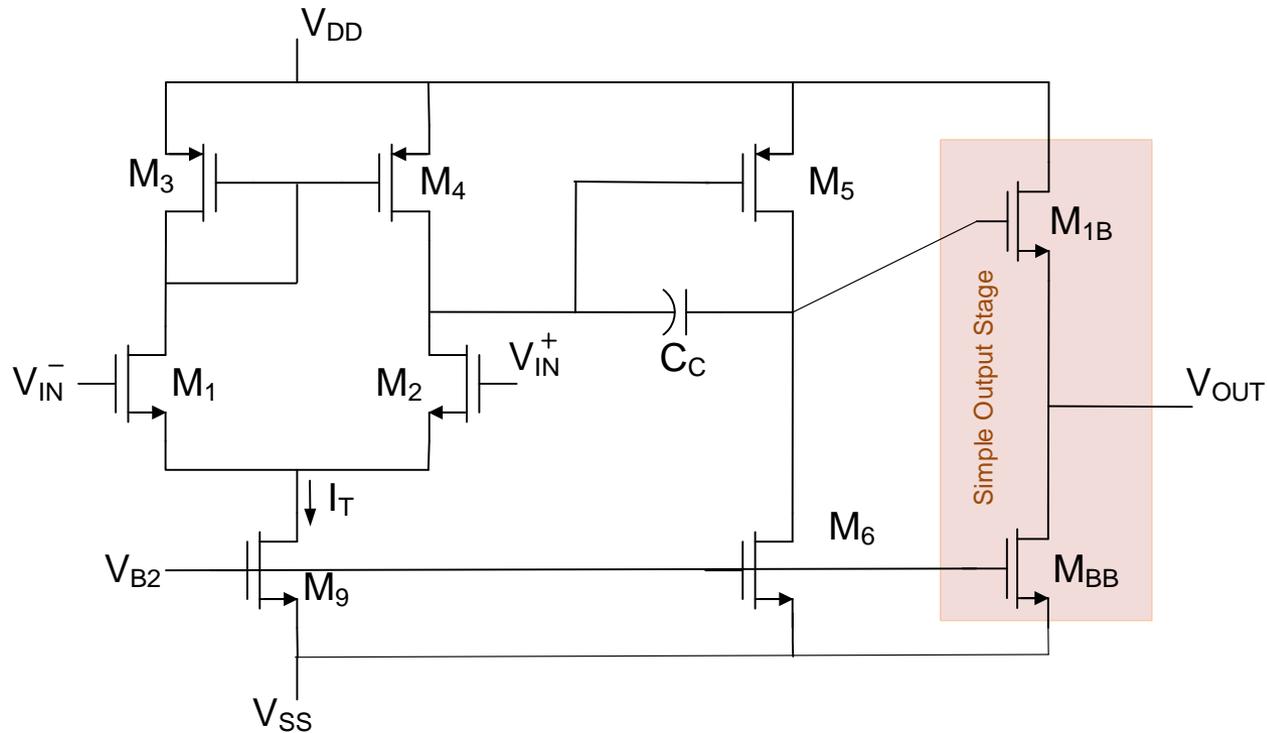
# Output Stages



- Recognized as Common Drain Amplifier
- Termed a Class A Amplifier
- Excellent Frequency Response
- Low Output Impedance and High Input Impedance
- Simple
- Output Signal Swing Reduced
- Power Dissipation in Class A Amplifiers Typically Considered Large



# Output Stages

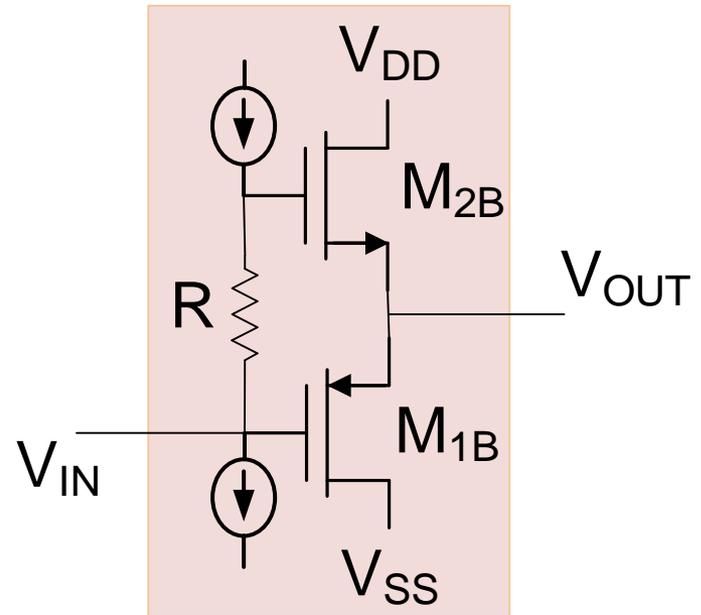
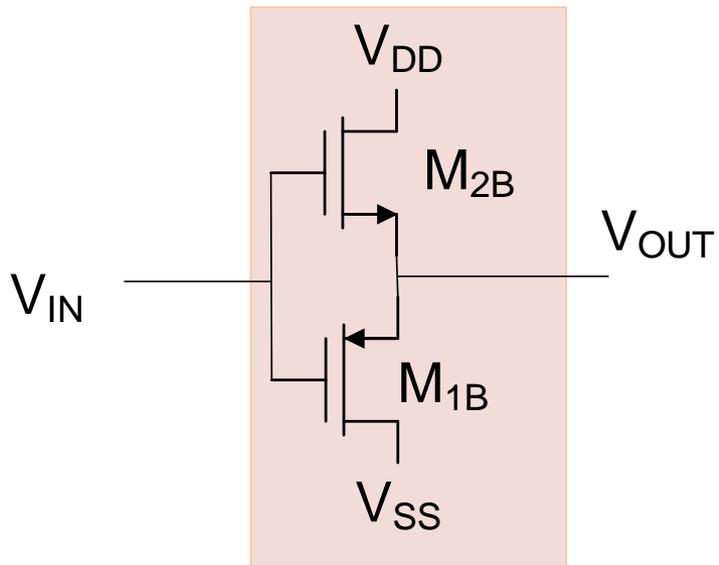


7T Op Amp with Output Stage

Technically 3-Stage but Pole of Output Stage at High Frequencies so often classified as two-stage

Note  $C_C$  often comes from output of second stage but could come from  $V_{OUT}$

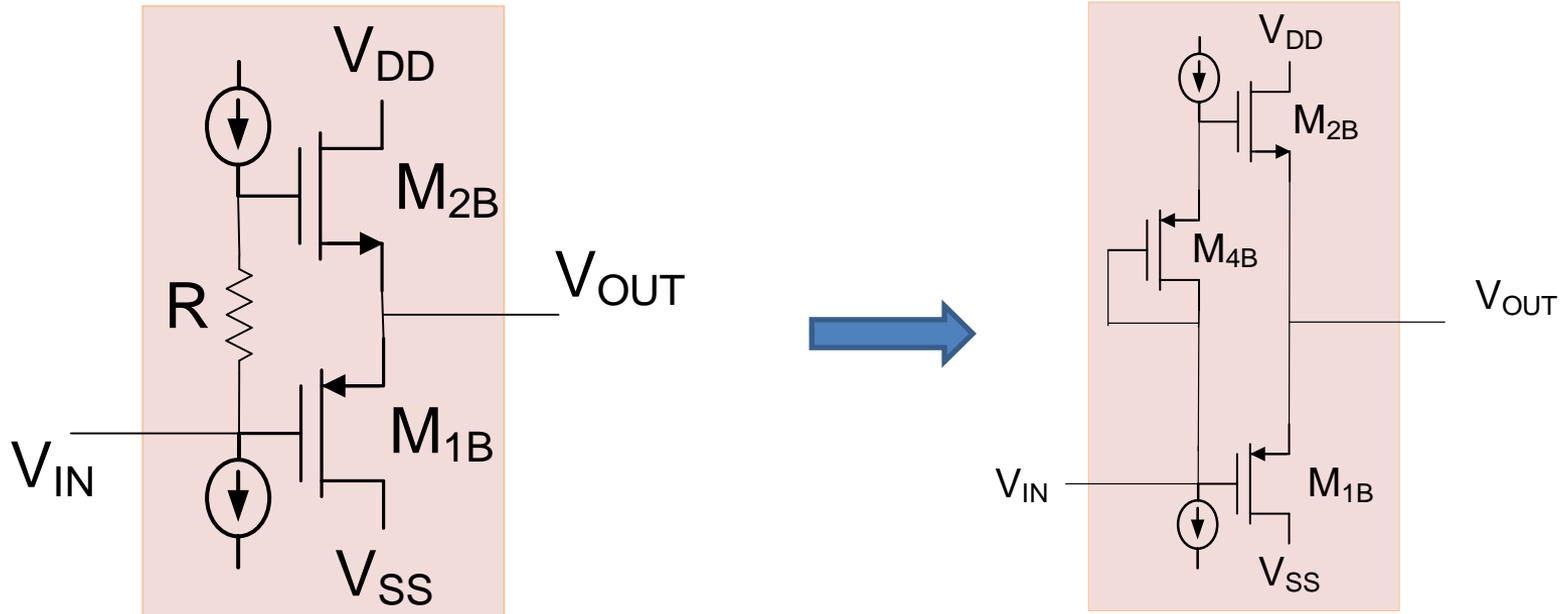
# Other Output Stages



- Push-Pull
- Class B
- Cross-over Distortion
- More power efficient at Low Output Levels

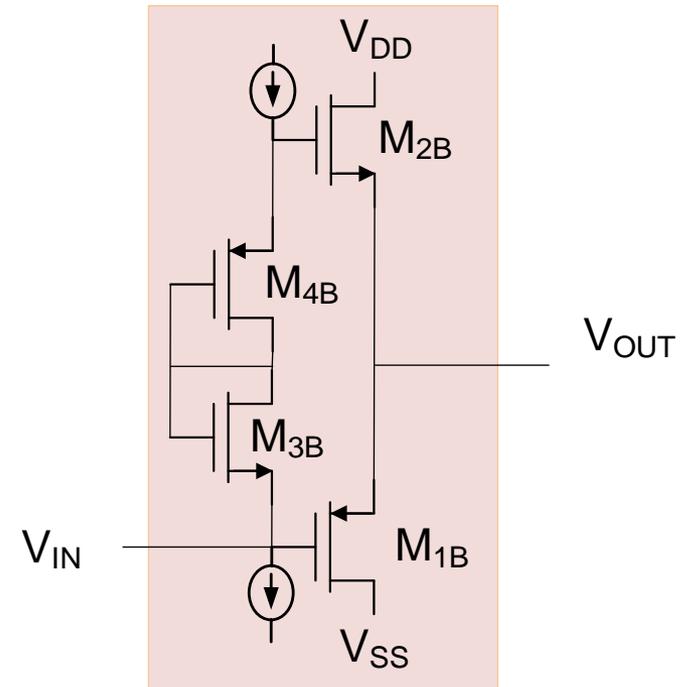
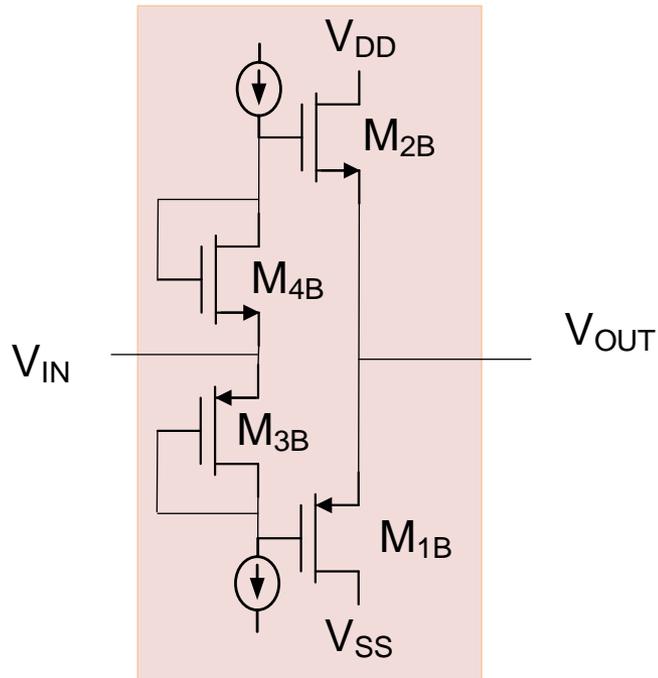
- Push-Pull
- Class AB
- Reduced Cross-over Distortion
- More power efficient at Low Output Levels than Class A

# Other Output Stages



- Push-Pull
- Class AB
- Reduced Cross-over Distortion
- More power efficient at Low Output Levels than Class A

# Other Output Stages



- Push-Pull
- Class AB
- Reduced Cross-over Distortion
- More power efficient at Low Output Levels than Class A



- Good luck on the final exam!
- Wishing all the best for the summer or the next step in your career

**Stay Safe and Stay Healthy !**

End of Lecture 44